

## Technote 9

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# A Starting Point for Insuring Op Amp Stability

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## A Starting Point for Insuring Op Amp Stability

A wise man once said to always “...add a feedback capacitor across  $R_f$  unless you can show that this capacitor isn’t necessary (or is doing more harm than good).”<sup>1</sup> A properly sized capacitor,  $C_f$ , placed across the feedback resistor in an Op Amp circuit can insure stability over a wide range of conditions with minimal effect on signal bandwidth. In this Technote, we will discuss the effects of input capacitance in Op Amp circuits and derive equations to properly size  $C_f$  compensate for non-idealities in feedback networks. Before we do, however, let’s start with a review of Op Amp terminology. I have found that there can be significant confusion regarding the various “gains” that are important when designing with Op Amps<sup>2</sup>.

What makes Op Amps so universal is that there are a set of standard configurations that can be “programmed” by a few external components forming the feedback network. This simplicity makes Op Amps attractive to designers, but it can also lull them into complacency. The feedback network is described by the feedback factor,  $\beta$ , given by:

$$\beta = \frac{R_g}{R_g + R_f} \quad (1)$$

The feedback factor is typically treated as being purely resistive, but more accurately, and critical to this discussion, it should be written as:

$$\beta = \frac{Z_g}{Z_g + Z_f} \quad (2)$$

Note that  $\beta$  is always less than or equal to 1<sup>3</sup>. The closed-loop or -3 dB bandwidth of an Op Amp circuit is given by:

$$f_{CL} = f_{\tau} \beta \quad (3)$$

where  $f_{\tau}$  is the gain-bandwidth product of the Op Amp. This is another way of saying that the product of the closed-loop bandwidth and the closed-loop gain ( $1/\beta$ ) of the amplifier is a constant that we call the gain-bandwidth product ( $GBW$ ) of the Op Amp.

$$f_{3dB} \frac{1}{\beta} = f_{CL} A_{CL} = f_{\tau} = GBW \quad (4)$$

Another name for closed-loop gain is noise gain, which is always defined as the reciprocal of the feedback factor. A common error is to use signal gain in place of closed-loop gain or noise gain in calculations. The signal gain of an Op Amp circuit is not always the same as its noise gain. The signal gain can be the inverting or non-inverting gain, depending on the configuration (or both in a difference amplifier). This is why I advocate the use of the term noise gain because it is not ambiguous. The noise gain, combined with the open-loop gain ( $A_v$ ) is what determines in large part the performance of the amplifier. The product of these terms is called the loop gain ( $A_v \beta$ ).

Phase Margin, a measure of the stability of the amplifier, is the difference between the phase of  $A_v \beta$  and  $-180^\circ$  at the frequency where  $|A_v \beta| = 0$  dB. The condition for oscillation is

<sup>1</sup> This quote is credited to Bob (Robert A.) Pease, formerly of National Semiconductor, acknowledged analog design guru, and self-proclaimed “Czar of Bandgaps”, although I have no doubt a similar phrase has been said by many of the analog design gurus consigned to history.

<sup>2</sup> Reference “*Technote 6 - Opamp Definitions*” and “*Technote 7 - Using Op Amps Successfully*” for more details.

<sup>3</sup> In an email, Bob Pease pointed out that while this is the typical case, there are special cases “where gain is in the feedback path: (1) using a grounded-base transistor as a logger, and (2) when you have to add a booster amplifier to get more drive or swing”. Did I mention there is no substitute for many, many years of experience?

given by  $A_v\beta = 1 \angle \pm 180^\circ$ , and there is an inverse relationship between the phase margin and the amplitude of the overshoot (and corresponding ringing) in the step response of an amplifier. Figure 1 graphically summarizes these terms.

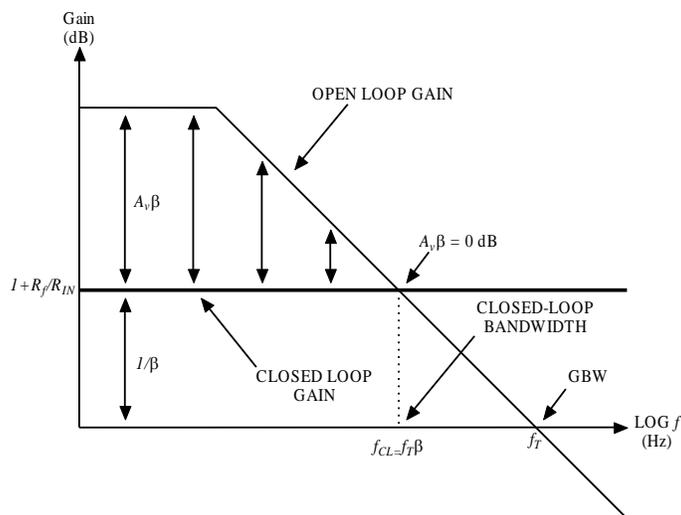


Figure 1: Op Amp Open Loop Gain and Closed-Loop (Noise) Gain

It should be clear from our discussion so far that introducing a pole in the feedback factor, and thus an additional pole in  $A_v\beta$ , also puts a zero in the noise gain. This reduces the phase margin, increases the overshoot in the step response, decreases the stability of the amplifier, and possibly results in the amplifier oscillating.

It turns out that there is always a zero present in the noise gain. The question is whether it is located above or below  $f_{cl}$  and how much it will degrade the phase margin. Primarily, three things influence the location of this zero<sup>4</sup>. First, if the Op Amp is driving a capacitive load the interaction of the Op Amp output impedance and the load capacitance will form a pole in  $\beta$  (a zero in the noise gain,  $1/\beta$ ) and decrease the phase margin. This Technote won't address this case because remediation usually involves several different design choices and designers are typically aware of unique conditions established by the load<sup>5</sup>. This Technote focuses on the second factor, the feedback factor pole created by the interaction of the feedback network with the input capacitance of the circuit. This pole is present in all designs to varying degrees because all Op Amps have input capacitance. In bipolar devices it may only be a few pF, but in JFET or CMOS amplifiers it can easily reach 15 -30 pF. Third, , sometimes designers add input capacitance to the Op Amp circuit by implementing a differentiator or, more commonly, interfacing a photodiode to a transimpedance amplifier<sup>6</sup> (TIA). In this case,  $C_{IN}$  can range from tens of pF to nF's or more. The frequency of the zero in the noise gain is given by:

$$f_z = \frac{1}{2\pi(R_f \parallel R_{IN})C_{IN}} \tag{5}$$

<sup>4</sup> In truth, there can be multiple zeros but, as designers, we should really try to avoid doing lots of dumb things simultaneously.

<sup>5</sup> But then, I often give designers more credit than I should. Driving even small capacitive loads requires forethought.

<sup>6</sup> An excellent starting point for this unique class of amplifiers is "Noise Analysis of FET Transimpedance Amplifiers", Texas Instruments, SBOA060 (aka Burr Brown AB-076). Then move on to "Building Electro-Optic Systems: Making It All Work" by Phillip C.D. Hobbs for a more complete presentation of the issues.

Placing  $C_f$  across  $R_f$  introduces a zero in the feedback factor (which is a pole in the noise gain) and correspondingly introduces a zero in the loop gain ( $A_v\beta$ ). The frequency of the pole in the noise gain is given by:

$$f_p = \frac{1}{2\pi R_f C_f} \tag{6}$$

Adding  $C_f$  increases the phase margin and improves the stability of the amplifier. Figure 2 summarizes the response when  $C_{IN}$  and  $C_f$  are present. But if  $C_f$  is too large it can limit the amplifier bandwidth, and too large a phase margin slows the step-response and settling time. Thus, it would be best if a value of  $C_f$  was determined by something other than random selection. Fortunately, this is easily done, but a little more information is needed.

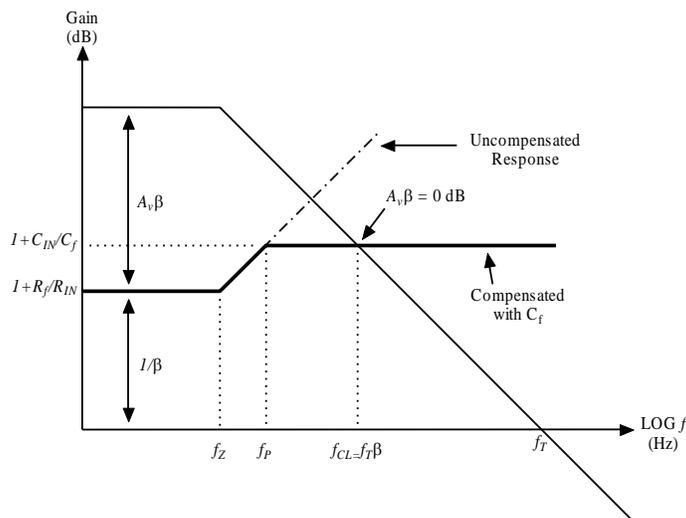


Figure 2: Noise gain showing effects of input and feedback capacitance

What Figures 1 and 2 neglect to show is that all Op Amps have additional poles in  $A_v$ . For a fully compensated ( $A_{CL} = 1$  stable) Op Amp, the second pole is located at or slightly above  $f_T$ . So in practice, we are starting with at least  $-90^\circ$ , and more likely  $-110^\circ$  to  $-135^\circ$  of phase shift, so there is not a lot of margin left in  $\beta$  before the step-response of the amplifier is unusable. In general, selecting  $R_f$  and  $R_{IN}$  for high gain works in our favor. High gain shifts  $f_{CL}$  lower in frequency and the Op Amp's second pole has less influence where  $|A_v\beta| = 0$  dB (unity loop gain). But Equation (5) shows that if large values are selected for both  $R_f$  and  $R_{IN}$ , the zero will be located at lower frequencies, and the phase margin will be degraded.

Using Equation (2) and computing the noise gain  $1/\beta$  shows that if the noise gain is low and  $C_{IN}$  is small,  $A_{CL} = 1 + R_f/R_{IN}$ . However, more often than not the noise gain peaks to  $1 + C_{IN}/C_f$  at higher frequencies, especially if  $C_{IN}$  or  $R_f \parallel R_{IN}$  is "large". This is typically the case with transimpedance amplifiers. In the past, a general rule was to make  $C_{IN} = C_f$  to limit the peaking to 6 dB. In the absence of any other knowledge it's not a bad rule, but with TIA's it frequently results in the signal bandwidth being limited excessively. However, it is not an optimum approach because it doesn't address the specific locations of the pole and zero in the noise gain, so it's likely you could increase the bandwidth and/or phase margin with a more analytical approach. Keep in mind that total noise is given by the integration under the noise gain response, so more peaking means a lot more noise.

A final note before we discuss optimizing the selection of  $C_f$ : I usually have my students perform a lab where they build a non-inverting amplifier using a ‘741-type Op Amp, and configure the feedback network with identical resistor values; sequentially using pairs of 1 k $\Omega$ , 10 k $\Omega$ , 100 k $\Omega$ , 1 M $\Omega$ , and 10 M $\Omega$  resistors. Of course, this is before I tell them to always include a small feedback capacitor. “Theory”, or at least the relationships given in Equations (1) and (3), says the closed-loop gain should be +2 and the bandwidth around 500 kHz as long as the ratio of the resistors is preserved, regardless of their absolute size. Reality is quite different. With resistor pairs as low as 100 k $\Omega$ <sup>7</sup> the zero given in Equation (5) rapidly moves into the passband and results in significant peaking in the noise gain. With pairs of 1 M $\Omega$  the amplifier is nearly useless and at 10 M $\Omega$  there a lot of oscillators running in the lab.

Moving on to the optimization of  $C_f$ , I recently reread “*Troubleshooting Analog Circuits*” by Robert A. Pease (I highly recommend the book). I came across a section that talked more about sizing  $C_f$  and gave specific equations. However, Pease didn’t give the background behind the equations and only stated that “I won’t bore you with the math...” I trust Bob because he is good and a conscientious engineer, but I know enough about design to realize that everything is a trade-off. If you don’t understand the basis for a rule, you really don’t understand the trade-offs you may be forcing into your design. That’s not my style. As it turns out, the math is quite simple, so here it is.

The first case discussed is for “high values of gain and  $R_f$ ”. In this situation, the peaking in the noise gain is  $1 + C_{IN} / C_f$ . If the gain is high this is  $\approx C_{IN} / C_f$ . Equating the frequency of the noise gain pole introduced by  $C_f$  with the closed-loop bandwidth yields:

$$\frac{1}{2\pi R_f C_f} = f_\tau \frac{C_f}{C_{IN}} \quad (7)$$

Solving for  $C_f$  yields:

$$C_f = \sqrt{\frac{C_{IN}}{2\pi f_\tau R_f}} \quad (8)$$

In the book, the “ $2\pi$ ” in the denominator is missing, but I’m confident that it’s a typo<sup>8</sup>. I would also argue that this case should be expanded to include amplifiers with high values of  $C_{IN}$  and/or high values of  $R_f \parallel R_{IN}$ . Essentially, Equation (8) is trying to address the case where the gain is moderate to high and a zero is present in the noise gain at a frequency below  $f_{CL}$ , which will cause peaking in the response as  $A_v\beta \rightarrow 0$  dB if left uncompensated. The compensation pole frequency is chosen to stop the rise in the noise gain near the intersection with the open-loop gain curve. The result insures a phase margin of 45° to 90° and the amplifier is unconditionally stable. Under these circumstances Equation (8) yields a good starting point for a design.

The next case addressed is when the “gain or impedance is low” and is given by the condition:

<sup>7</sup> The situation is exacerbated by the stray capacitance in the “white board”-type of prototyping boards commonly used.

<sup>8</sup> So much for being confident. I traded emails with Bob Pease and he said he leaves the  $2\pi$  out deliberately so that he can then “trim the capacitor downward if you need a little more bandwidth.” That makes sense. He also mentioned his “gimmick” where you make a capacitor from a pair of twisted wires. You can untwist or clip off some of the length to reduce the capacitance of your “gimmick”. I first learned of this technique from reading “Pease Porridge” and have used it. It works well.

$$1 + \frac{R_f}{R_{in}} \leq 2 \sqrt{2\pi f_\tau R_f C_{IN}} \quad (9)$$

Again, I added the  $2\pi$  inside the radical as it is another typo in the book. The basis for this equation is not intuitively obvious. However, playing with some algebra transforms it to:

$$\frac{1}{2\pi(R_f \parallel R_{IN})C_{IN}} \leq 4f_\tau \frac{R_{IN}}{R_f + R_{IN}} \quad (10)$$

What this equation means is that for this condition, the zero in the noise gain is at a frequency no larger than about 4 times  $f_{CL}$ . This makes sense because, if it is out at a frequency much higher than that, it doesn't have a significant effect on the phase margin. This case is more common than many people realize, particular with high-bandwidth and FET or JFET input amplifiers. The approach in this case is to put the pole at a frequency twice that of the zero, or:

$$\frac{1}{2\pi R_f C_f} = 2 \frac{1}{2\pi(R_f \parallel R_{IN})C_{IN}} \quad (11)$$

Solving for  $C_f$  yields:

$$C_f = \frac{C_{IN}}{\left(2 + 2 \frac{R_f}{R_{IN}}\right)} \quad (12)$$

This can be rewritten as:

$$C_f = \frac{C_{IN}}{2} \frac{R_{IN}}{R_f + R_{IN}} \quad (13)$$

Equations (8) and (13) will yield good starting point values for  $C_f$ . In his book, Pease goes on to emphasize that what I have referred to above as “rules” are really only guidelines. You will need to perform additional measurements on your amplifier to make sure that you have sufficient phase margin and stability. Did you catch that? You need to build the amplifier and test it to see if the performance meets the requirements. Never, ever, rely solely on spice<sup>9</sup> to design an amplifier. Spice is a useful tool for experienced engineers<sup>10</sup>, but it requires a healthy dose of skepticism when examining the results. Only a fool thinks the output from spice is always true or even true beyond a limited set of assumptions. And when you build your circuit, don't test only with sinusoids. Sine waves are “nice” because they don't stress a circuit the way a pulse will. Input small and large signal pulses and look at the step response of the amplifier. It will allow you to directly compute the phase margin from the overshoot. Pease likes to apply square waves to the output of an amplifier through “a couple hundred ohms in series with a 0.2  $\mu$ F capacitor” and with various capacitive loads. Try it. It will tell you a lot about how your amplifier can be expected to operate in the wild. Of course, you have already performed a full AC analysis by hand before you started, so nothing you see at the bench will surprise you, right?

<sup>9</sup> Or any other simulator.

<sup>10</sup> Pease's writings are very negative regarding spice. However I think he is more upset with lazy engineers who believe anything a computer tells them than with the program itself. I believe that in the hands of a skeptic who understands what spice actually does and knows that spice can lie with an incredibly straight face, it can be a useful tool. Unfortunately, too many engineers use it as a crutch, thus lending support to Pease's opinion.