Reset Noise in Multiplexed Photodiode Arrays

by

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In situations where a multiplexed photodiode array is not background shot noise limited, the dominant source of noise is typically reset noise, also referred to as *kTC* noise. Reset noise results from the interaction between the FET used to reset the photodiode and video line to the reference voltage, and the capacitance of the video line, photodiode, and preamplifier input circuitry. Figure 1 shows a typical multiplexed photodiode array readout circuit, such as that found in a Reticon® S-series linear array. The phase clocks are used to propagate a voltage introduced by the START pulse, sequentially activating the multiplex switches and sharing the charge on the photodiode integration capacitance, C_p, with the video line capacitance, C_v. The reset FET switch is activated at the end of the readout cycle for each photodiode, reinitializing the photodiode capacitance for the next integration and readying the video line to read out the next photodiode.

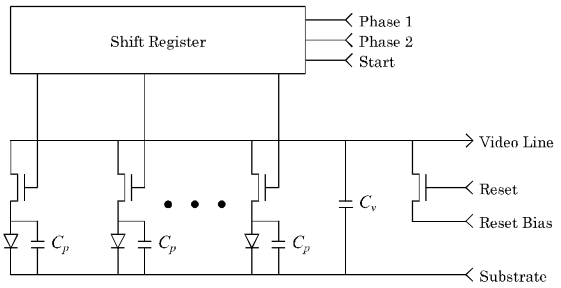

Figure 1. Typical multiplexed array readout architecture

Reset noise results from the Johnson noise associated with the reset FET channel resistance. Conceptually, this can be viewed as an uncertainty introduced in the reset level as a result of the thermal noise present on the video line. The typical model used for deriving the magnitude of the reset noise is shown in Figure 2.

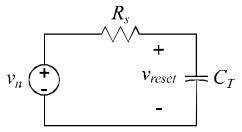

Figure 2. Model for deriving magnitude of reset noise

The Johnson noise voltage, v_n, associated with FET reset switch resistance, R_s, is given by:

$$v_n = \sqrt{4kTR_s\Delta f} \tag{1}$$

Where k is Boltzmann's constant (1.38×10^{-23} W sec K^{-1}), T is temperature in degrees Kelvin, and Δf is the electrical bandwidth in Hz. The dynamic switch resistance and the total array output capacitance, C_T, combine to limit the noise equivalent bandwidth of the system to:

$$\Delta f = \frac{p}{2}\cdot\frac{1}{2pR_sC_T} \tag{2}$$

Note that the total array output capacitance is given by the sum of the photodiode capacitance, the video line capacitance, the preamplifier input capacitance, C_a, and any stray capacitance, C_s, associated with the layout of the circuit.

Substituting equation (2) into equation (1) yields the expression for the reset noise voltage, v_{reset}.

$$v_{reset} = \sqrt{\frac{kT}{C_T}} \tag{3}$$

Using the relationship between the charge and voltage on a capacitor, $Q = CV$, the rms noise charge on the video line, Q_{reset}, can be derived as:

$$Q_{reset} = \sqrt{kTC_T} \tag{4}$$

Hence the name *kTC* noise. Q_{reset} can be converted to electrons, the more common unit of measure, by dividing by the electronic charge (1.6×10^{-19} coulombs/electron).

It is interesting to note that the FET switch resistance does not influence the magnitude of the noise, only the noise bandwidth. Using a Reticon® RL0512S linear array with a Burr-Brown® OPA627 preamplifier and external

Siliconix® SD211 reset switch[1] as a baseline, and assuming T = 300 K, the following values can be obtained:

$$C_p = 2 \text{ pF}$$
$$C_v = 12 \text{ pF}$$
$$C_a = 15 \text{ pF}$$
$$C_s = 1 \text{ pF}$$
$$R_{off} = 10^{10} \ \Omega$$
$$R_{on} = 50 \ \Omega$$

Using the above equations and noting that C_T = 30 pF, the following results are obtained:

$$Df_{on} = 416.7 \text{ MHz}$$

$$Df_{off} = 0.833 \text{ Hz}$$

$$v_{reset} = 11.75 \ \mu\text{V}$$

$$Q_{reset} = 2203 \text{ electrons}$$

The large change in the noise bandwidth between the "on" and "off" states of the reset switch should permit the correlated portion of the reset noise to be removed from the video output signal. This technique is referred to as correlated double sampling (CDS). The CDS circuit uses a capacitor to store the video line voltage at the instant just after the reset switch turns off, and then subtracts this voltage from the value of the next photodiode integrated onto the video line. This configuration is shown in Figure 3.

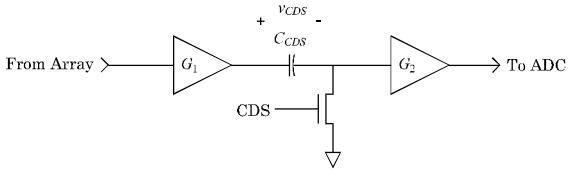

Figure 3. Typical correlated double sampling architecture

Just after the reset portion of the array readout, the CDS switch is turned on and the array output voltage is stored on C_{CDS}. This voltage is a composite of several sources, including the offset voltage on the output of the array (and subsequent amplifier stages), the charge injected onto the video line by the reset switch, and the value of the reset noise at the time the reset switch changed states. It also includes contributions from the other noise sources in the system, such as the preamplifier, noise on the array bias, etc. The CDS switch is turned off just prior to the multiplexer switching the next photodiode onto the video line. At this time, the voltage remaining on C_{CDS} is subtracted from the voltage produced by the next photodiode. In addition to canceling the correlated noise, CDS serves to restore the DC reference level (or other reference level if the CDS switch is tied to a voltage other than ground) of the video signal.

The reason this configuration is able to sample the reset noise is due to the change in the noise bandwidth between "on" and "off" states of the reset switch. As shown above, in the "on" state, the reset noise equivalent bandwidth exceeds 400 MHz, which is undoubtedly greater than the bandwidth of the readout electronics. However, when the switch closes, the reset noise equivalent bandwidth drops to less than 1 Hz. This effectively "locks in" the reset portion of the noise on the video line because the rate of change of the noise voltage is now so severely limited that any change during the photodiode readout period is negligible.

When implementing CDS, the storage capacitor must be sized carefully so as to preserve system performance. There are two constraints which have to be observed. First, the upper limit for C_{CDS} is established by the drive capabilities of the amplifier preceding the CDS circuit. During the CDS reset noise sampling period t_s, the drive amplifier has to be able to charge the capacitor fast enough to settle v_{CDS} to less than 1/2 the value of the least-significant bit (LSB) of the downstream analog-to-digital converter (ADC). The voltage, v_{CDS} , on the CDS capacitor is given by:

$$v_{CDS} = V_o\left[1 - e^{-\left(\frac{t_S}{R_{on}C_{CDS}}\right)}\right] \qquad (5)$$

V_o is the output voltage of CDS drive amplifier and R_{on} is the FET switch on resistance. Since we desire $V_o = v_{CDS}$, the error in the above equation is given by the exponential term. Taking into account the gain, G_2, between the CDS circuit and the ADC, the upper bound on C_{CDS} is given by:

[1]An external reset switch is frequently used in place of the internal switch because of the high "on" resistance exhibited by the internal FETs.

$$C_{CDS} \le \frac{t_s}{R_{on}} \left[\ln\left(\frac{2^{N+1} G_2 V_o}{V_{FS}} \right) \right]^{-1} \qquad (6)$$

Where V_{FS} is the full scale input range of the ADC and N is the ADC resolution in bits. Note that V_o can be obtained from the gain G_1 between the array and the CDS, and the offset voltage out of the array, V_{offset}, using:

$$V_o = G_1\left(V_{offset} \pm a v_{reset} \right) \qquad (7)$$

The scale factor a represents the rms to peak conversion factor (typically 3 to 4). Typically, $V_{offset} >> a v_{reset}$, so equation (6) reduces to:

$$C_{CDS} \le \frac{t_s}{R_{on}} \left[\ln\left(\frac{2^{N+1} G_1 G_2 V_{offset}}{V_{FS}} \right) \right]^{-1} \qquad (8)$$

Depending on the array biases, V_{offset} may range from a few millivolts to 5 volts. Typical values for V_{FS} range from 2.5 volts to 10 volts.

The lower limit on C_{CDS} is established by looking at the droop, Δv_{CDS}, on the capacitor during the photodiode readout, or hold, period. The droop is given by:

$$\Delta v_{CDS} = \frac{t_h\left(i_{bias} + i_{leak} \right)}{C_{CDS}} \qquad (9)$$

Where t_h is the CDS hold period, i_{bias} is the downstream amplifier bias current, and i_{leak} is the CDS FET switch leakage current. It is necessary to keep the error contributed by Dv_{CDS} less than 1/2 LSB. Substituting the value of the LSB and solving for C_{CDS} yields:

$$C_{CDS} \le \frac{2^{N+1} t_h G_2 \left(i_{bias} + i_{leak} \right)}{V_{FS}} \qquad (10)$$

The problem with the above approach to reset noise cancellation is that the original reset noise model, shown in Figure 2, does not completely represent the reset noise in the system. As a result, the CDS topology implemented does not completely eliminate reset noise. This has been confirmed by the various systems developed using Reticon® readouts. In every case, the dark level noise performance has been six to seven times the calculated reset noise level when CDS is not implemented, and approaches the calculated reset noise level when CDS is implemented. Tests have shown that the noise level in both cases tracks directly the square root of the total array output capacitance, thus eliminating the possibility that other noise sources are dominant. There are (at least) four possible explanations for this discrepancy, however, the following discussion reveals that additional study is required to fully explain the performance obtained.

The first area of study has to do with reset noise carryover from the previous scan. The following is the sequence of events which occurs during the readout of a photodiode in the array. $P_{n,j}$ is used to denote photodiode n of frame j. When the multiplexer switch for $P_{n,j}$ closes, the integrated charge on the photodiode capacitance is redistributed to the total array output capacitance. At the end of the readout period, the reset switch closes while the multiplexer switch is still closed, reinitializing $P_{n,j}$ and the video line. When the reset switch opens, reset noise voltage on the video line is sampled by the CDS. Note, however, that this same reset noise level remains on $P_{n,j}$. The multiplexer then advances to the next photodiode, $P_{n+1,j}$, and the CDS differences the signal from $P_{n+1,j}$ and the reset noise sample stored from $P_{n,j}$. Thus, the conventional approach to CDS removes the reset noise due to the video line and preamplifier input capacitance but permits the pixel to carry the reset noise voltage to the next frame, where it is differenced with an uncorrelated reset noise sample. Unfortunately, this cannot explain the large noise levels seen in the designs described above. When $P_{n,j+1}$ is read, the noise voltage remaining from $P_{n,j}$ is scaled by the ratio C_p/C_T. Because this ratio is typically ≥ 10, the magnitude of this affect is small.

Another possible noise source has to do with the off-state multiplexer switches. When $P_{n,j}$ is being read out, there are anywhere from 127 to 511 (depending on array length) additional multiplexer switches attached to the video line, and all are noise sources as described by equations (1) through (4). While the bandwidths of the noise voltages are low, the magnitudes are high. Also, the spectra of the reset noise associated with the multiplexer switches exhibits a bandpass characteristic, where that associated with the reset

FET is a lowpass function. The significance of this is currently unknown.

The stability of the video line and photodiode capacitance could also contribute to the errors in the signals read from multiplexed arrays. In these multiplexed arrays, it has been observed that the capacitance of the clock inputs is a function of the applied voltage. If similar effects are exhibited by the video line and photodiode capacitance, then the noise levels being sampled by the CDS would no longer be correlated, or be only partially correlated, and would significantly reduce the effectiveness of the CDS technique. This also requires study.

The final area of investigation, which is frequently blamed by the authors in this area for the poor performance of these devices, is bias noise. Two paths exist for this type of interference in the system. First, the reference used for the reset FET can couple noise onto the video line. Typically, analog ground is used for this purpose, but depending on the array technology used, this could be a voltage reference. Second, noise could be associated with the bias applied to the substrate of the array. The substrate would appear to be the most likely problem area, since the photocurrent shares the substrate with the various clock return currents. It is difficult to conclude, however, that this is the dominant noise source in the system. As described above, the noise levels obtained track C_T, and the mechanism by which bias noise could exhibit this effect is not known. Further study in this area is also needed.

At this point, it should be obvious that much associated with the ultimate performance level obtained from multiplexed photodiode arrays is still not well understood. Because advances in this area will have a significant impact on the spectroscopy and remote sensing communities, we are in the process of developing a LDRD (Laboratory Directed Research and Development) proposal to try to enhance our understanding of the noise phenomena and to develop new approaches to processing the video signals. Several analog and digital signal processing architectures have been proposed that could be used to replace the conventional CDS and will, in all probability, improve the noise performance of these systems. However, the cost of extracting the information necessary to further reduce reset noise is usually increased complexity and power consumption. Rather than take what is essentially a shotgun approach to this problem, the LDRD proposal is being structured so that a greater understanding of the noise sources is developed and graduated system concepts are produced which trade cost, complexity, and power consumption with performance. Eventually, it would be desirable to integrate these architectures on monolithic structures to further control the parameters effecting system performance.