Preliminary Tests of a High Efficiency 1-D Silicon Pixel Array for Small Angle Neutron Scattering

W.J. McNeil, S.L. Bellinger, B.J. Blalock, C.L. Britton, Jr., J.L. Britton, S.C. Bunch, S.A. Cowley, C.M. Henderson, T.J. Sobering, R.D. Taylor, D.S. McGregor

Abstract-A first generation 120 micron pitch pixel array system for neutron detection using the PATARA amplifier chip was assembled and tested. The pixel array was tested for neutron response and spatial resolution. Pulses from the PATARA were observed at 0.5 V in height and 500 ns wide from neutron interactions. The spatial resolution of the array was determined to be 119 micrometers. Leakage current tests and alpha particle irradiation tests were conducted for a second generation prototype silicon sensor with 175 micrometer deep perforated trench structures in each pixel. The second generation sensor incorporates several design improvements to ease fabrication.

I. INTRODUCTION

Gas detectors are commonly used for neutron scattering experiments. High neutron counting efficiency and tightly spaced anode structures allow for good counting statistics and relatively small spatial resolution. The special resolutions of gas detector arrays are commonly on the order of mm, such that the spatial resolution is limited by the range of the reaction products in the gas. To achieve high neutron counting efficiency with a gas conversion medium, the detectors must be relatively large, thereby reducing the response time of the detectors, thereby limiting the detector counting rates. This problem can be reduced by using a solid neutron conversion medium in the ionization chamber, as was done for the MicroMegas detector system [1].

Solid state neutron detectors, such as thin film conversion devices, offer the advantage of much smaller spatial resolution and higher counting rates than current gas detector arrays. The planar array design easily accommodates micron scale structures. Also, the short ranges of the reaction products, being tens of μ m, allow for the fabrication of much smaller pixels and the realization of shorter charge carrier drift lengths, hence improving both spatial resolution and response time. However, the neutron counting efficiency of thin film planar devices are limited to less than 5% [2]. Thicker films would increase this efficiency, but the ability to count events diminishes when the thickness of the film exceeds the range of the charged particle reaction products. Planar devices can be double-sided or stacked to improve efficiency up to approximately 8% [2]. Nevertheless, the low efficiency limitation has reduced their usefulness in applications such as neutron imaging.

Recently, non-planar perforated semiconductor devices have been developed that incorporate solid neutron conversion material into the bulk of the device. These devices are fabricated by etching deep perforations through a *pn* junction diode detector and subsequently backfilling the perforations with neutron reactive material. These perforated diodes have demonstrated intrinsic thermal neutron counting efficiency up to 35% to date [3]. The dramatic increase in efficiency draws interest to perforated detectors for solid state imaging systems. Described in the following work is a first effort to apply perforated neutron detector technology into a simple linear pixel array for neutron scattering experiments.

A 1-D pixel array is being designed specifically for small angle neutron scattering (SANS) experiments to be performed at the spallation neutron source (SNS) at Oak Ridge National Laboratory. To meet the experiment requirements, an array has been designed and fabricated on silicon with pixels 100 μ m wide and 4 centimeters long. It is planned to build a device with at least 1000 pixels, each with a 100 μ m pitch. This work describes only the first generation prototype system that includes 32 pixels with a pitch of 120 μ m and readout electronics composed of two 16 channel PATARA amplifiers [4]. The PATARA ASIC was designed specifically for the large neutron flux expected at the SNS and the High Efficiency Neutron Detector Array (HENDA). The performance of the 1-D silicon pixel array is briefly discussed.

II. SENSOR DESIGN

N-type float zone silicon with resistivity 10-20 k Ω -cm was chosen for substrate material to allow for deep depletion with modest bias requirements. Using a boron nitride solid source diffusion process to make shallow p-type junctions, full depletion through the wafer thickness is achieved with reverse bias less than 30 volts. Yet, the built-in junction potential, in most cases, allows for the full energy of charged particles to

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W.J. McNeil (e-mail: wjm4444@ksu.edu), S.L. Bellinger, C.M. Henderson, S.A. Cowley, D.S. McGregor USA (telephone: 785-532-5284, e-mail: mcgregor@ksu.edu) are with the SMART Lab. of Kansas State Univ., Manhattan, KS 66506.

B.J. Blalock is with the Electrical Engineering Department, University of Tennessee, Knoxville, TN USA (email:bblalock@utk.edu).

C.L. Britton, Jr., is with the Electrical Engineering Department, University of Tennessee, Knoxville, TN USA, and also with ORNL, Oak Ridge, TN, USA (e-mail: brittoncl@ornl.gov).

J.L. Britton was with the Electrical Engineering Department, University of Tennessee, Knoxville, TN USA, and is now at Texas Instruments Inc., Knoxville, TN (e-mail: j-britton@ti.com).

S.C. Bunch was with the Electrical Engineering Department, University of Tennessee, Knoxville, TN USA, and is now at Ametek Inc., Oak Ridge, TN (e-mail: scbunch@gmail.com).

T.J. Sobering, R.D. Taylor are with the Electronics Design Lab. of Kansas State Univ., Manhattan, KS 66506 USA. (e-mail: edl@ksu.edu).

be collected with no externally applied bias. This reduces the electronics power requirements on the system motherboard.

The relatively low total neutron cross-section and a low Znumber of Si reduces image blurring and detector sensitivity to gamma-rays. High aspect ratio dry etching techniques (for deep vertical perforation structures) and effective surface passivation methods have been well developed for Si; therefore, Si is an ideal material for the HENDA.

A. Pixel Layout

The first generation prototype array utilizes p-type diffused regions 100 μ m wide and 4 cm long, each separated by 20 μ m. Aluminum metal contacts line the perimeter of each pixel and minimize resistance along the pixel length. The aluminum metal contact traces connect the pixels to the 125 μ m square bonding pads. A staggered design maximizes trace-to-trace distances and better matches the pitch of the PATARA amplifier chip (see Fig. 1).

Metal traces the periphery of each pixel so that deep trenches could be etched through the middle region of the pixel without complex multilayer etch processes. However, for the first generation prototype, a thick film of ⁶LiF was evaporated uniformly over the entire array and no etching was performed.

Fabrication and testing of the first prototype revealed many improvements necessary for the second generation design. An array with a smaller pitch of 100 μ m was designed and fabricated with larger alignment tolerances and larger bonding pads. The second generation array includes etched trenches 30 μ m wide and over 100 μ m deep within each pixel (see Fig. 2).

B. Readout Electronics

The PATARA amplifier combines a preamplifier, shaper, and baseline restorer in one package. Additional features include adjustable gain, adjustable leakage current compensation and switchable polarity. The first generation utilizes 16 channels and a global discriminator adjustment. Two amplifiers were installed on the first generation prototype, each reading out the even or odd pixels of the 32 pixel array.



Fig. 1. First generation pixel array design utilizing traces to bonding pads extending over the silicon dioxide, with a uniform ⁶LiF film coating over all pixels.



Fig. 2. The second generation array design has rounded structures, larger bonding pads without traces, and most importantly, deep etched trenches within each pixel. These trenches are to be backfilled with ⁶LiF and coated uniformly with a ⁶LiF film.

III. RESULTS

The first generation prototype system has been completely assembled and tested for response to neutrons, including pulse captures and a spatial resolution test on the 32 channel array. The second generation prototype system has yet to be assembled, but preliminary bench-top testing of the sensor array has been performed. This includes leakage current and alpha particle testing before ⁶LiF application.

A. Signal Formation

A typical pulse from the PATARA output during neutron irradiation has (roughly) a 0.5 volt peak height and 0.5 μ s width. The observed SNR and the narrow pulse width assure that counting rates exceeding 10^5 cps per pixel are achievable with manageable dead time (or pulse pile-up).



Fig. 3. Typical neutron event pulse observed at output of the PATARA amplifier. The 0.5 V pulse height and 0.5 μs width are very suitable for high count rates.

B. Spatial Resolution

After centering the 32 channel array in a neutron beam from the TRIGA Mark II nuclear reactor at Kansas State University, the global LLD settings of each PATARA were adjusted to give the most uniform and similar response between the odd and even pixels of the array. An evaporated Gd straight edge mask was mounted on a tilting and translating stage and placed in front of the array to cover approximately half of the pixels. The Gd straight edge was aligned along a single pixel length. A trial and error process was performed first tilting and then re-centering the mask to achieve the best alignment of the mask to the array. When the sharpest edge response was obtained, the mask was considered aligned.



Fig. 4. Knife edge response from an evaporated Gd mask translated over three pixels of the array. A good error function fit and derived Gaussian reveals 119 micrometer spatial resolution.

The mask was then translated across the array at 25 μ m increments to provide enough data points to observe a smooth edge response function. Fitting an error function to the data and numerically differentiating produced a Gaussian point spread function with a FWHM of 119 μ m.

C. Second Generation Bench Top Testing

Leakage current and alpha particle response of the pixel array were tested on a probe station. The leakage current of a diode is expected to increase after dry etching deep structures in the substrate, primarily due to the creation of interface states on the surfaces of the etched structure. Work has been performed, successfully, to minimize leakage current in perforated structures [5]. In the present case, the leakage current increased after dry etching, but not excessively (Fig. 5).



Fig. 5. Leakage current increase for the perforated diode design, showing the difference before and after the dry etch step. At present, a leakage current increase of less than one order of magnitude is acceptable for operation.

Device depletion was tested with an alpha particle source. Alpha particle spectra collected from ²⁴¹Am clearly show that

the energy deposited by alpha particles, as a function of increasing voltage in the depleted region, increases from partial to full deposition. Fig. 6 indicates that the depletion volume of the device is increasing beyond the alpha particle range in the silicon.



Fig. 6. A shift in the energy peak of alpha particles from ²⁴¹Am indicate an increase in the volume of the depleting device.

IV. CONCLUSION

A solid-state neutron detector array system has been tested and demonstrates impressive, yet expected, results. The 119 μ m spatial resolution and fast timing response shows clear advantages over gas detector arrays presently in use. Considering a single pixel area (0.04 cm²) and assuming a thermal neutron detection efficiency of 20%, one can expect reliable measurement results for neutron fluxes up to 10⁸ n cm² s⁻¹. Overall, these devices should work well for neutron imaging.

REFERENCES

- [1] C.L. Britton, Jr., W.L. Bryan, A.L. Wintenburg, R.J. Warmack, T.E. McKnight, S.S. Frank, R.G. Cooper, N.J. Dudney, G.M. Veith, and A.C. Stephen, "A Detector for Neutron Imaging," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 3, pp. 1016-1019, June, 2004.
- [2] D.S. McGregor, M.D. Hammig, H.K. Gersch, Y-H. Yang, and R.T. Klann, "Design Considerations for Thin Film Coated Semiconductor Thermal Neutron Detectors, Part I: Basics Regarding Alpha Particle Emitting Neutron Reactive Films," *Nucl. Instrum. and Meth.*, A500, pp. 272-308, 2003.
- [3] W.J. McNeil, S.L. Bellinger, E.L. Patterson, J.K. Shultis, C.J. Solomon, T.C. Unruh, and D. S. McGregor, "Angular Response of Perfoated Diode High Efficiency Neutron Detectors," *IEEE. NSS Conf. Record*," submitted, Nov. 2007.
- [4] J.L. Britton, S.C. Bunch, C.L. Britton, D.S. McGregor, and L. Crow, "PATARA: Solid-State Neutron Detector Readout Electronics with Pole-Zero and Complex Shaping and Gated Baseline Restorer for the SNS," *IEEE NSS Conf. Record.*, vol. 1, pp. 27-31, Oct. 2006.
- [5] W.J. McNeil, S.L. Bellinger, T.C. Unruh, E.L. Patterson, J.K. Shultis, and D.S. McGregor, "Perforated Diode Fabrication for Neutron Detection," *IEEE NSS Conf. Record.*, vol. 6, pp. 3732-3735, Oct. 2006.