A GRINDING-BASED MANUFACTURING METHOD FOR SILICON WAFERS: GENERATION MECHANISMS OF CENTRAL BUMPS ON GROUND WAFERS

Wangping Sun  
Department of Manufacturing & Mechanical Engineering  
Technology, Oregon Institute of Technology, Klamath Falls, Oregon, USA

Z. J. Pei  
Department of Industrial and Manufacturing Systems Engineering, Kansas State University, Manhattan, Kansas, USA

Graham R. Fisher  
MEMC Electronic Materials, Inc., St. Peters, Missouri, USA

Most integrated circuits (IC) are fabricated using silicon wafers. The continuing shrinkage of the size of IC features has imposed more and more stringent requirements on the wafer flatness. Furthermore, wafer manufacturers are under constant pressure to reduce the wafer cost. The traditional lapping-based manufacturing method is unable to satisfy the ever-increasing demand for better flatness and lower cost. Previous experimental study of a grinding-based manufacturing method has shown that excellent site flatness can be obtained on ground wafers except for a few sites at the wafer center. One cause for the poor flatness at the wafer center is the central bumps on the ground wafers. As a follow-up, this paper investigates the generation mechanisms of the central bumps on ground wafers, and provides solutions to eliminate or reduce them. The understanding and knowledge gained through this study can also be applied to the manufacturing of other semiconductor wafers (such as germanium, gallium arsenide, and silicon carbide).

Keywords Central Bump, Central Dimple, Lapping, Semiconductor Material, Silicon Wafer, Silicon Wafer Grinding, Wafer Flatness

INTRODUCTION

The advancement in computer, telecommunication, and internet technologies demands faster and smaller integrated circuits (IC) (1). The IC features have continuously shrunk since the beginning of semiconductor fabrication. They started at about 125 \( \mu \text{m} \) in the early 1950s (2) and reached 90 nm recently (3). The long-term average annualized reduction...
rate in feature sizes is projected to continue at approximately 11% (4). The feature sizes will reach 70 nm by 2007, and 20–35 nm by 2012–2016 (5).

Wafer flatness directly impacts device line-width capability, process latitude, yield, and throughput (6, 7). Continuing reduction in feature sizes demands increasingly flatter wafers (8). With the lapping-based method (currently the dominant manufacturing method), it is very difficult to manufacture silicon wafers with super flatness at a lower cost (9).

A grinding-based manufacturing method has demonstrated its potential to manufacture flat silicon wafers at a lower cost (9). An experimental investigation on the grinding-based method has shown that, except for a few sites at the wafer center, the site flatness of ground wafers can meet the stringent specifications for future silicon wafers. One cause for the poor flatness at the wafer center is the central bumps on ground wafers. This paper, for the first time in public domain, investigates the generation mechanisms of the central bumps. Based on the understanding obtained through the study, it also provides solutions to eliminate or reduce the central bumps.

There are six sections in this paper. Following this introduction section, we provide the background information, followed by analyzes the generation mechanisms of the central bumps on ground wafers. Then, computer simulations and experimental results are presented and compared, and solutions to eliminate or reduce central bumps are discussed next, followed by the conclusions.

**BACKGROUND INFORMATION**

**Grinding-Based Method for Silicon Wafer Manufacturing**

Figure 1 shows a grinding-based manufacturing method for silicon wafers. It includes the following major processes:

![Diagram of grinding-based manufacturing method for silicon wafers](image)

**FIGURE 1** A grinding-based manufacturing method for silicon wafers.
- Slicing: to slice a silicon ingot into wafers of thin disk shape;
- Grinding: to achieve a high degree of parallelism and flatness on the wafer;
- Rough polishing: to obtain a mirror surface on the wafer;
- Fine polishing: to obtain final mirror surface.

Note that some processes (e.g., edge grinding, edge polishing, laser marking, and final cleaning) are omitted in Figure 1 for simplicity. More information on wafer manufacturing processes is available in the literature (10–13) and at www.memc.com.

**Wafer Grinding**

A key process for the grinding-based manufacturing method for silicon wafers is wafer grinding (shown in Figure 2). For wafer grinding, the rotation axis for the grinding wheel is offset by a distance of the wheel radius relative to the rotation axis of the wafer. During grinding, the wafer is held on a porous ceramic chuck by means of vacuum. The grinding wheel and the wafer rotate about their own rotation axes simultaneously while the wheel is fed towards the wafer along its axis.

The ceramic chuck is typically ground to a conic shape with a very small slope, as shown in Figure 3. When the wafer is held onto the chuck,
it elastically deforms to the chuck’s conic shape, thus ensuring that the grinding wheel only contacts half of the wafer. This contact area is marked as “Active grinding zone” in Figure 2. Note that the localized elastic deformation of the grinding wheel near the wafer center is not taken into consideration here. As shown later, the localized elastic deformation of the wheel is the cause for the central dimples and bumps on the ground wafers.

**Poor Flatness at the Wafer Center after Grinding**

An experimental investigation (9) on the grinding-based manufacturing method for silicon wafers has shown that the site flatness of ground wafers can meet the stringent specifications for future silicon wafers, except for a few sites at the wafer center. There are two commonly seen irregularities on ground wafers: central dimples and central bumps, as shown in Figures 4 and 5 respectively. These two figures are the printouts of UltraGage 9500 (more information about the instrument can be found later). Typically, for a silicon wafer with a diameter of 200 mm, its thickness is about 0.75 mm. The size of a central dimple ranges from 10 mm to 30 mm in diameter and less than 0.2 μm in depth. The size of a central bump also ranges from 10 mm to 30 mm in diameter and less than 0.2 μm in height.

The central dimples and bumps adversely affect the site flatness at the wafer center. Their elimination is critical to the success of the grinding-based manufacturing method for silicon wafers. However, it will be very difficult, if not impossible, to eliminate them if their generation mechanisms are unknown. This study is the first attempt (in the public domain) to understand the generation mechanisms of the central bumps on ground wafers and, based on this understanding, to provide solutions to eliminate or reduce the central bumps.
FIGURE 4 A ground wafer with a central dimple.

FIGURE 5 A ground wafer with a central bump.
GENERATION MECHANISMS OF CENTRAL BUMPS ON
GROUND WAFERS

Generation Mechanisms of Central Dimples on Ground Wafers

The hypothesis for the generation mechanisms of central dimples is as follows. During grinding, due to the grinding force, the portion of the grinding wheel segment that is in contact with the silicon wafer (i.e., the portion of the wheel segment that is within the active grinding zone) will elastically deform. This deformation will cause the portion of the wheel segment that is next to the active grinding zone to contact with (cut into) the silicon wafer near the wafer center (on the opposite side of the active grinding zone). The cutting action of this portion of the wheel segment (outside the active grinding zone) will remove the material from the silicon wafer near the wafer center, in addition to the material removed by the portion of the wheel segment within the active grinding zone, causing the central dimple. More detailed explanation on the generation mechanism of central dimples is available in an earlier publication (14).

Based on this hypothesis, Zhang et al. (14) developed a finite element analysis model to predict the relationships between the dimple size and the influencing factors (including the chuck shape, the grinding force, and the mechanical properties and geometry of the grinding wheel segment). Pilot experiments were conducted and the experimental results were consistent with the model predictions.

The above discussion is based on the assumption that the ceramic chuck is perfectly flat or has a conic shape with straight surfaces (i.e., there is no dimple at the chuck center). However, as illustrated next, there could be a dimple at the chuck center depending on the grinding conditions when the chuck is ground.

Generation Mechanisms of Central Dimples on Ceramic Chucks

In industry, the ceramic chuck is prepared by a grinding process almost identical as the wafer grinding. Comparing to the grinding wheels for grinding silicon wafers, the grinding wheels used for grinding ceramic chucks typically have larger diamond grit sizes and a “harder” bond system (Young’s modulus is larger). Sometimes, metal-bond wheels are used for grinding ceramic chucks (instead of resin-bond wheels for grinding silicon wafers).

The hypothesis for the generation mechanisms of central dimples can be used to explain that there may be central dimples on ceramic chucks. Even though the central dimples on ceramic chucks cannot be experimentally observed due to the limitation of the measuring instrumentation (15),
accepting the presence of central dimples on ceramic chucks results in a plausible explanation for the existence of central bumps on ground wafers that are observable experimentally.

**Generation Mechanisms of Central Bumps on Ground Wafers**

As discussed in the preceding sections, when certain conditions are met, a central dimple (with the depth of $h_{\text{chuck}}$ and the radius of $r_{\text{chuck}}$) will

![Diagram](image)

$r_{\text{chuck}}$, $h_{\text{chuck}}$: radius and depth of the dimple on the chuck (formed when the chuck is ground).

$r_{\text{wafer}}$, $h_{\text{wafer}}$: radius and depth of the dimple on the wafer front surface (before the wafer is taken off from the chuck).

(a) A central dimple is generated on the front surface of a ground wafer before the wafer is taken off from the chuck with a central dimple

(b) A central bump is generated on the ground wafer after the wafer is taken off from the chuck with a dimple (when the dimple on the chuck is deeper than the dimple on the wafer front surface)

**FIGURE 6** Generation mechanisms of central bumps on ground wafers (the depths of the central dimples and central bump are greatly exaggerated for illustration purpose).
be generated on the ceramic chuck. When a wafer is ground on the chuck with a central dimple, a central dimple (with the depth of \( h_{\text{wafer}} \) and the radius of \( r_{\text{wafer}} \)) will be generated on the front surface of the wafer (before the wafer is taken off from the chuck). After the wafer is removed from the chuck, a central bump may be present on the final wafer shape of the ground wafer if the central dimple on the chuck is deeper than the central dimple on the front surface of the wafer (before the wafer is removed from the chuck). Note that the final wafer shape is defined as the shape of the wafer front surface when the wafer back surface is assumed to be flat. This definition is consistent with the wafer thickness map used on ADE’s Ultra-Gage, which is the measurement tool used for this study, and also the most-widely used flatness gage in industry.

The generation mechanisms of central bumps on ground wafers are further illustrated in Figure 6. When a wafer is ground on a chuck with a central dimple, due to the vacuum pressure (through the porous ceramic chuck) and the grinding force, the wafer will elastically deform to conform to the chuck shape. As a result, the central dimple on the chuck will be filled with the silicon material during grinding. Using the finite element analysis, Liu et al. (16) reported that the elastic deformation of the wafer caused by the grinding force was about 8 times larger than that caused by the vacuum. Therefore, it is plausible for the wafer to elastically deform to fill the central dimple on the ceramic chuck.

The above discussion can also be used to explain the generation mechanisms of central dimples on ground wafers when the wafers are ground on a chuck with a central dimple. If the depth of the dimple on the chuck is smaller than the depth of the dimple on the wafer front surface (before the wafer is removed from the chuck), there will be a dimple on the final shape of the ground wafer after the wafer is removed from the chuck.

**COMPUTER SIMULATIONS AND GRINDING EXPERIMENTS**

**Computer Program and Simulation Results**

Based on the understanding presented above, a computer program was developed using MatLab (The MathWorks, Inc., Natick, MA) to simulate the central irregularities (i.e., central dimples and central bumps) on ground wafers. The structure of the simulation program is shown in Figure 7. The program first gets the radii of the dimples on the chuck and on the wafer front surface (before the wafer is removed from the chuck) from the finite element analysis (FEA) model for central dimples (14). It also gets the assumed depths of the dimples on the chuck and on the wafer front surface (before the wafer is removed from the chuck).
Note that the actual depths of the dimples cannot be measured due to the limitations of available measurement tools (15). The program then obtains the ideal chuck shape and the ideal wafer front surface from the wafer shape model (17). Next, it modifies the central areas of the ideal chuck shape and the ideal wafer front surface using the data representing the dimple on the chuck and the dimple on the wafer front surface (before the wafer is removed from the chuck). Finally, the final wafer shape is calculated and plotted.

Figures 8 and 9 show nine simulated final wafer shapes for 200 mm wafers. It can be seen that the wafer will be flat if the dimple on the chuck and the dimple on the wafer front surface (before the wafer is removed from the chuck) are identical (i.e., $r_{\text{chuck}} = r_{\text{wafer}}$ and $h_{\text{chuck}} = h_{\text{wafer}}$). Otherwise either a central dimple or a central bump will exist on the ground wafer.

It can also be found that the depth of the dimple on the chuck (formed during the chuck preparation) relative to the depth of the dimple on the wafer front surface (formed during wafer grinding and before the wafer is removed from the chuck) determines what surface irregularity will appear on the ground wafer. If $h_{\text{chuck}} < h_{\text{wafer}}$, there will be a central dimple on the ground wafer; if $h_{\text{chuck}} > h_{\text{wafer}}$, there will be a central bump on the ground wafer.

**Grinding Experiment Conditions and Results**

Single crystal silicon wafers of 200 mm in diameter with the (100) plane as the major surface (the front or back surface of the wafer) were used for
To ensure the consistency of test wafers, all wafers were lapped using the same lapping conditions prior to grinding. Grinding experiments were conducted at Strasbaugh Inc. (San Luis Obispo, CA) on a model 7AF wafer grinder. The grinding wheels used were diamond cup-wheels. The radius of the wheels was 140 mm. The grit size for the coarse grinding wheel was mesh #320. The grit size for the fine grinding wheels was mesh #2000. Fine wheels with different values of Young’s modulus were used.

$r_{\text{chuck}}$, $h_{\text{chuck}}$: radius and depth of the dimple on the chuck (formed when the chuck is ground).

$r_{\text{wafer}}$, $h_{\text{wafer}}$: radius and depth of the dimple on the wafer front surface (before the wafer is taken off from the chuck).

Note: The edge part of the wafer has been clipped to magnify the central part. In other words, the central portion of the wafer shown in the table is only 50 mm in diameter, although the wafer diameter is 200 mm.

FIGURE 8 Three-dimensional views to show the central irregularities on ground wafers (after the wafers are taken off from the chuck).
Most wafers were ground using the conditions listed in Table 1. Note that there were three feed rate values, used for three sequent steps, respectively. During grinding, deionized (purified) water was used to cool the grinding wheel and the wafer surface. The coolant was supplied to the inner side of the cup wheel, at a flow rate of 11.4 l min\(^{-1}\) (or, 3 gal min\(^{-1}\)). Different

\( r_{\text{chuck}}, h_{\text{chuck}} \): radius and depth of the dimple on the chuck (formed when the chuck is ground).

\( r_{\text{wafer}}, h_{\text{wafer}} \): radius and depth of the dimple on the wafer front surface (before the wafer is taken off from the chuck).

FIGURE 9 Cross-sectional views to show the central irregularities on ground wafers (after the wafers are taken off from the chuck).

---

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Coarse grinding</th>
<th>Fine grinding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removal</td>
<td>µm</td>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td>Wheel speed</td>
<td>rev s(^{-1})(rpm)</td>
<td>32.05 (1923)</td>
<td>72.50 (4350)</td>
</tr>
<tr>
<td>Chuck speed</td>
<td>rev s(^{-1})(rpm)</td>
<td>1.67 (100)</td>
<td>9.83 (590)</td>
</tr>
<tr>
<td>Feed rate for step 1</td>
<td>µm s(^{-1})</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Feed rate for step 2</td>
<td>µm s(^{-1})</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Feed rate for step 3</td>
<td>µm s(^{-1})</td>
<td>0.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>
chuck shapes were used for the experiments. Due to limitations of available measurement tools (15), the exact chuck shapes were not known. However, it is possible to know approximately the actual chuck shape from the chuck shape predicted from the mathematical model developed earlier (15, 17) based on the setup parameters used for grinding the chuck.

<table>
<thead>
<tr>
<th></th>
<th>ADE graphs from grinding experiments</th>
<th>Computer simulations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Central dimple</td>
<td><img src="image" alt="Central dimple ADE graph" /></td>
<td><img src="image" alt="Central dimple computer simulation" /></td>
</tr>
<tr>
<td>Central bump</td>
<td><img src="image" alt="Central bump ADE graph" /></td>
<td><img src="image" alt="Central bump computer simulation" /></td>
</tr>
<tr>
<td>No dimple, no bump</td>
<td><img src="image" alt="No dimple, no bump ADE graph" /></td>
<td><img src="image" alt="No dimple, no bump computer simulation" /></td>
</tr>
</tbody>
</table>

**FIGURE 10** Comparison of experimental results and computer simulations.
Central dimples and central bumps were measured on a flatness gage, Model UltraGage 9500 (ADE Corporation, Westwood, MA). More information on UltraGage 9500 can be found at www.ade.com. Figure 10 compares the experimental results with the computer simulations. The matches between the experimental and simulation results are reasonably good. The experimental conditions are listed in Table 1, and the simulation parameters are listed in Table 2.

### TABLE 2  Simulation Parameters and Their Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Central dimple</th>
<th>Central bump</th>
<th>No dimple, no bump</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_{\text{chuck}}$</td>
<td>mm</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>$h_{\text{chuck}}$</td>
<td>μm</td>
<td>0.5</td>
<td>1.2</td>
<td>0.5</td>
</tr>
<tr>
<td>$r_{\text{wafer}}$</td>
<td>mm</td>
<td>13</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>$h_{\text{wafer}}$</td>
<td>μm</td>
<td>1.0</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

$r_{\text{chuck}}, h_{\text{chuck}}$: radius and depth of the dimple on the chuck (formed when the chuck is ground). $r_{\text{wafer}}, h_{\text{wafer}}$: radius and depth of the dimple on the wafer front surface (before the wafer is taken off from the chuck).

Solutions to Eliminate or Reduce Central Bumps

So far, it has been shown that a central dimple can be generated not only on the wafer front surface but also on the chuck. Unless these two dimples are identical, there will be central irregularities on ground wafers. In practice, the chuck is typically made of porous ceramic material (different from silicon). Therefore, the dimple on the chuck and the dimple on the wafer front surface (before the wafer is removed from the chuck) are almost always different.

This finding reveals a solution to eliminate the central bumps and central dimples altogether: use silicon (or a material that has similar mechanical properties to silicon) to fabricate the chuck. In this way, the depth and radius of the dimple on the chuck and the depth and radius of the dimple on the wafer front surface (before the wafer is removed from the chuck) will be the same (or very close to each other) if the same grinding wheel and grinding conditions are used to grind the chuck and the wafer.

There are additional benefits to use silicon (or a similar material) to fabricate the chuck. It may make it possible to eliminate the adjustment of spindle angles to produce flat wafers. A major reason to adjust the spindle angles is that the chuck material is different from silicon and, therefore, the grinding force when grinding the chuck is different from that when grinding the wafers. Further discussion on spindle angle adjustments can be found in other papers (18, 19).
Furthermore, central bumps can be reduced if the central dimple on the ceramic chuck and the central dimple on the wafer front surface (before the wafer is removed from the chuck) are reduced. According to Zhang et al. (14), the following measures can effectively reduce the central dimples on ground wafers (and similarly, on ground ceramic chucks):

1. Use a conic-shaped chuck with a sufficiently large slope.
2. Use a grinding wheel with a more rigid segment (larger Young’s modulus, larger width and smaller height for the wheel segment).
3. Use grinding conditions that minimize the grinding force (for example, to select a lower feed rate).

CONCLUSIONS

This paper reports an investigation into the generation mechanisms of central bumps on ground wafers. It also provides some practical solutions to address this critical issue in the grinding-based manufacturing method for silicon wafers. The major conclusions are as follows:

1. Central dimples can be formed on both the ceramic chuck and the wafer front surface (before the wafer is removed from the chuck) when they are ground. The relative sizes (depths and radii) of these two dimples determine what the wafer center will be: flat, a dimple, or a bump.
2. The wafer center will be flat only if the dimple on the chuck and the dimple on the wafer front surface (before the wafer is removed from the chuck) are identical \( r_{\text{chuck}} = r_{\text{wafer}} \) and \( h_{\text{chuck}} = h_{\text{wafer}} \). If \( h_{\text{chuck}} < h_{\text{wafer}} \), there will be a dimple on the ground wafer; if \( h_{\text{chuck}} > h_{\text{wafer}} \), there will be a bump on the ground wafer.
3. The central bumps and central dimples can be reduced or eliminated by using a steeper chuck shape, selecting a more rigid grinding wheel, and choosing grinding conditions that has lower grinding forces.

The knowledge gained through this study can be applicable to the manufacturing of other semiconductor wafers, such as germanium, gallium arsenide, and silicon carbide.

ACKNOWLEDGMENTS

This material is based upon the work supported by the National Science Foundation under Grant No. 0348290 (CAREER Award). Financial support was also provided by the Advanced Manufacturing Institute of 14 W. Sun et al.
Kansas State University. The authors would like to thank Mr. Salman Kassir at Strasbaugh, Inc. (San Luis Obispo, CA) for his assistance in conducting the grinding experiments.

REFERENCES


