

Technote 7

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Using Op Amps Successfully

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Op Amps are extremely useful and fairly simple devices. However, the basic ideal model presented in typical Circuit Theory and Electronics classes can trick most students into believing they understand these devices. In reality, while you have been taught more than you realize, what is needed is for you to make a few more connections between the facts and methods you have learned.

Let's start by reviewing the basics. Op Amps are high-gain DC coupled amplifiers usually intended to amplify signals over a wide frequency range. They have a differential input and a single-ended output. This is illustrated in Figure 1.

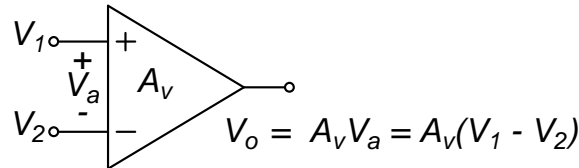


Figure 1. Op Amp in an "open-loop" configuration

You have already been exposed to a set of ideal assumptions that make it quite easy to analyze an Op Amp circuit. For example, you have been taught that A_v , the open-loop gain¹, is infinite. Initially this sounds confusing because if the gain is infinite, shouldn't the output voltage be infinite as well? How is this device useful? In reality, Op Amps work because they are always configured so the output will "drive" the input differential voltage nearly to zero. This is called negative feedback and is the key to making Op Amps so useful. In your classes you were probably taught about "virtual ground"² or told that the voltage between the Op Amp's inputs is zero. This is what was being described to you. Keep this concept in mind as it helps in the analysis, as I will show later.

Figure 2 illustrates a more detailed but still simplified model for a voltage feedback³ Op Amp. Table 1 summarizes the remaining ideal Op Amp assumptions. Some of these terms may be unfamiliar to you so I will try to clarify each of these characteristics. What is

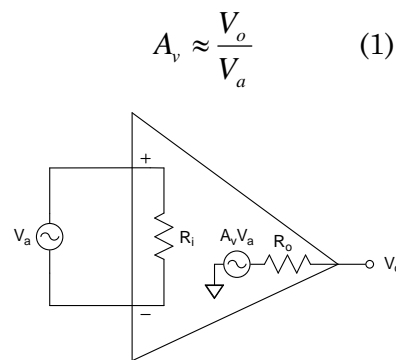


Figure 2. Op Amp Equivalent Circuit

Ideal Characteristic	Circuit Effect
No current flows in the inputs	$I_{bias(+,-)} = 0$ or $Z_{in} = \infty$
No output voltage for zero input	$V_{os} = 0$
Voltage gain is infinite	$A_v = \infty, V_a = 0$
Output impedance is zero	$Z_{out} = 0$
Frequency response is flat and infinite	$BW = \infty$ or Delay = 0 and $GBW = \infty$
Slew Rate is infinite	$BW = \infty$ or Delay = 0 and $GBW = \infty$
Infinite CMRR and CMR	Unlimited input voltage range. Differential response only
PSRR is infinite	Immune to PS offset and variations
Noise free	Output due to signal only

Table 1. Ideal Op Amp Characteristics

¹ This is the gain when there is no feedback to "close the loop". Depending on the reference this can also be designated as A_{OL} or possibly something different. Use caution to avoid confusion as it is a critical parameter.

² I do not like this term as "ground" really only applies in the inverting Op Amp configuration. It is better to think in terms of the inputs being driven to the same potential.

³ There are two types of Op Amps – Voltage Feedback and Current Feedback. They are similar but differ in critical points. Current Feedback Op Amps are not as common and generally used in high speed applications. They will not be covered in this document.

important at this point is that the ideal Op Amp assumptions make analyzing an Op Amp circuit trivial. Keep in mind that you should always start an analysis using the ideal assumptions. If the circuit does not work using an ideal analysis, there is no point in performing a more detailed analysis. It should be obvious that the ideal characteristics listed will be replaced later with real characteristics. However, often each characteristic can be examined individually to determine the effect on the actual circuit.

Figures 3 and 4 show the inverting and non-inverting Op Amp configurations. The impedances Z_i and Z_f “close the loop” and determine the “gain” of the circuit (in addition to other characteristics). Looking at Figure 3, the output voltage is “fed back” to the inverting input terminal. This provides the negative feedback discussed above⁴. Think in these terms: as the output voltage increases, the voltage at the inverting input (V_2 in Figure 1) increases (remember Superposition?), which causes the difference $V_1 - V_2$ to decrease, which causes the output to decrease. This is negative feedback.

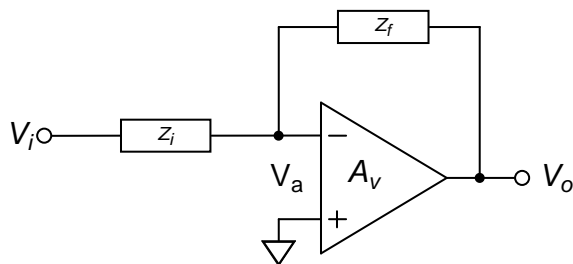


Figure 3. Inverting Op Amp Configuration

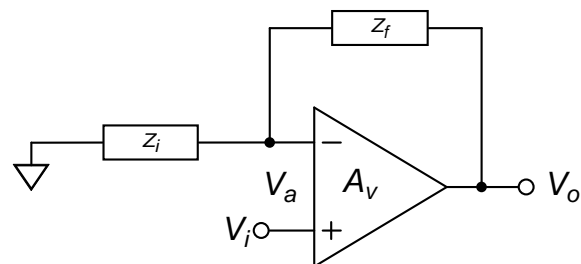


Figure 4. Non-Inverting Op Amp Configuration

How does this help? Again referring to Figure 3, because there is negative feedback, the output can drive the input differential voltage V_a to zero. Then the signal, or closed-loop, gain can be determined by applying KCL at the inverting input terminal.

$$\frac{V_i + V_a}{Z_i} + \frac{V_o + V_a}{Z_f} = 0 \quad (2)$$

Keep in mind that we are assuming that the Op Amp has infinite input impedance, which means no current flows into either input. Also, we are assuming that there is no DC error at the output (offset voltage $V_{os} = 0$ V). And, if the open-loop gain is infinite, $V_a = 0$ V. Equation (2) then simplifies to:

$$\frac{V_o}{V_i} = -\frac{Z_f}{Z_i} \quad (3)$$

The ideal analysis of the circuit in Figure 4 is similar. However, if $V_a = 0$ V, the voltage at the inverting input node must be V_i and the analysis yields:

$$\frac{V_o}{V_i} = 1 + \frac{Z_f}{Z_i} \quad (4)$$

⁴ The feedback connection in an Op Amp does not have to be made to the inverting input terminal. What is important is that the feedback voltage drives the output in the opposite direction. If there is “something” in the feedback loop that inverts the phase, the feedback would need to be to the non-inverting input.

What this means is that the (ideal) signal gain of an Op Amp circuit is determined only by the feedback network. For now I will skip over discussing the effects of non-infinite open loop gain (it will be discussed in detail below) and move on to the other ideal assumptions. However, notice that while the gain of the inverting configuration can assume (nearly) any value, the non-inverting configuration is limited to gains greater than one. In fact, a special case for the non-inverting configuration is when $Z_i \rightarrow \infty$. This is called a unity gain buffer or non-inverting voltage follower.

The input offset voltage (V_{OS}) is a DC error in the Op Amp and equals the voltage that needs to be added to the input to result in a zero volt output. It is usually a few microvolts to a few millivolts. Because of the high open loop gain of an Op Amp, this is never measured directly but instead, the Op Amp is configured as a non-inverting voltage follower (Figure 4 with $Z_i = \infty$ and $Z_f = 0 \Omega$) with V_i grounded. In this configuration, the output voltage equals V_{OS} . If you want to determine the effect of V_{OS} on the output voltage, it can be modeled as a voltage source in series with either the inverting or non-inverting input pin of the device. Eliminating this parameter by assuming it is zero slightly simplifies an analysis. However, the easiest way to include offset voltage in the analysis is to use superposition and analyze it separately. Thus, the contribution to the output voltage due to V_{OS} for the amplifiers in either Figure 3 or Figure 4⁵ is given by:

$$V_o|_{V_{OS}} = V_{OS} \left(1 + \frac{R_f}{R_i} \right) \quad (5)$$

Resistances are used as this is strictly a DC error. The polarity of V_{OS} is usually ignored as it is a function of the design and manufacturing and typically cannot be predicted.

The input bias current is the current flowing into or out of the input terminal. Bias currents are modeled as current sources from each input pin to ground and can range from femtoamps (for electrometer type Op Amps) to microamps. The direction of current flow is also a function of the design and manufacturing and cannot be predicted without some additional knowledge of the device. Again, eliminating bias currents makes the ideal analysis simpler, but it can be easily included again by using superposition. Referring to Figures 3 and 4 and assuming the bias current flows from ground to the input pin, the output voltage contributions are given by:

$$V_o|_{I_{BIAS-}} = -R_f I_{BIAS-} \quad (6)$$

$$V_o|_{I_{BIAS+}} = 0 \quad (7)$$

Again, resistances are used because this is a DC error. The contribution due to the non-inverting input bias current is zero because there is no resistance present for it to develop a voltage across. This is certainly the case in Figure 3. In Figure 4 this is problematic as V_i is most likely generated by a source having a source impedance. In this case, the contribution becomes:

$$V_o|_{I_{BIAS+}} = I_{BIAS+} R_s \left(1 + \frac{R_f}{R_i} \right) \quad (8)$$

⁵ When you apply superposition to compute the output contribution due to V_{OS} to the amplifiers in Figures 3 or 4, the circuits become identical.

This is the voltage induced on the source resistance times the DC gain of the amplifier. Figure 5 shows the Op Amp model including sources representing offset voltage and input bias currents. While it is starting to look more complicated, keep in mind that superposition can be used to greatly simplify calculating the contributions from each of these sources.

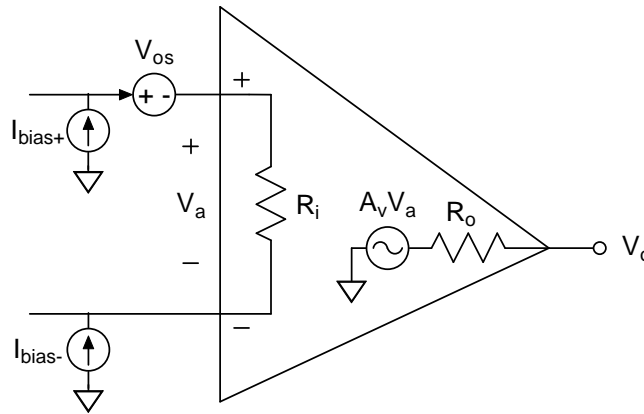


Figure 5. Op Amp model including common parameters.

It is possible to compensate for either input offset voltage or bias currents errors. However, caution must be used or additional problems can be created. In the case of V_{OS} , some Op Amps have offset null terminals and the data sheet will recommend a resistor network, usually including a potentiometer. The intention is to sum a voltage into the input stage and eliminate the offset voltage. My best advice is to never use these pins. First, potentiometers, while convenient, are notoriously bad devices having poor temperature characteristics and poor stability. Usually, these networks severely degrade the drift of the Op Amps (errors vs. temperature). As an alternative, it is possible to build an external network to sum a voltage into the circuit and eliminate the offset. However, the source must be very stable and temperature compensated. Usually this is not worth the effort. As a general rule, if V_{OS} is a problem, pick a better Op Amp.

Similarly, it is possible to compensate for input bias current. In Figure 3, if a resistor is added between the non-inverting input and ground with a value equal to $R_f || R_i$, the output voltage due to the bias currents is eliminated. This can be shown using Equation (8) and letting $R_s = R_f || R_i$.

$$V_o |_{I_{BIAS+}} = I_{BIAS+} \left(\frac{R_f R_i}{R_f + R_i} \right) \left(1 + \frac{R_f}{R_i} \right) = I_{BIAS+} R_f \quad (9)$$

This is equal to but of opposite polarity to the contribution due to I_{BIAS-} so they cancel. However, the addition of a bias current cancellation resistor can increase the noise at the output of the Op Amp. The problem is fixed by adding a capacitor in parallel with the bias current cancellation resistor to limit the noise bandwidth⁶.

The problem is more difficult with the circuit in Figure 4. Because it is likely that the source impedance driving V_i is low, it is difficult to make $R_s = R_f || R_i$. It is possible to add a

⁶ You are not expected to understand this at this time. "Noise" will have to be addressed later. Just keep in mind that you should not add a bias current compensation resistor without a parallel capacitor (1 μ F is usually sufficient).

series resistor at the non-inverting input such that $R_s + R_{series} = R_f || R_i$, but there is no good way to add capacitance to prevent the noise performance from being degraded.

Finally, there is one more consideration. The cancellation techniques discussed above assume the bias currents are both flowing in the same direction. However, it has become more common for manufacturers to add input circuitry to their Op Amps to try and reduce the magnitude of the bias currents. This can cause the bias currents to flow in different directions. The specification to watch is the input bias current offset, which is defined as the difference between the inverting and non-inverting bias currents. If the bias current offset is small compared to the bias current, it is safe to assume the bias currents flow in the same direction. However, if the magnitudes of the bias current and bias current offset are similar, there is no way to be sure that the inverting and non-inverting bias currents have the same direction and the techniques discussed above can actually make the problem worse. Generally, the best solution is to pick a better Op Amp with a lower bias current.

The remaining ideal assumptions from Table 1 are a little less obvious but useful none the less. For example, zero output impedance means that the Op Amp operates independently of the load impedance. In reality, the Op Amp has a finite drive capability and also the load impedance can be critical to the stability of the amplifier. This will be discussed later when open loop gain is revisited. The frequency response clearly cannot be flat and infinite (although with care the response of the amplifier can be flat out to a cutoff frequency). Op Amps have finite small signal bandwidth and in fact, this is where things get very interesting (again, more on this later). Slew rate is a large signal parameter and a measure of how fast (dV_o/dt) the output voltage can change. Op Amps vary widely in this respect from 0.5 V/ μ s to over 1000 V/ μ s.

CMR is common mode input range. CMRR is common mode rejection ratio. Common mode (CM) voltage is frequently misunderstood. Referring to Figure 1, the common mode voltage is defined as

$$V_{CM} = \frac{V_1 + V_2}{2} \quad (10)$$

As noted above, Op Amps are *differential* amplifiers; they are intended to respond only to the voltage difference between the input terminals. In Figures 3 and 4 above, this is how we analyzed the circuits. Note however that there is an important difference in these circuits. In Figure 3, the common mode voltage is zero. In Figure 4, $V_{CM} = V_i$. In the ideal model we assume this will have no effect. In reality, there are two considerations. First, there is a limit to how close the input can get to the power supply rails. This is the CMR and occurs because the input transistors of the Op Amp must remain properly biased for linear operation. Second, there is a contribution to the output voltage due to the common mode input voltage. This is the common mode gain; more commonly the reciprocal is used and referred to as the CMRR. CMRR is a function of frequency and is a measure of how well the Op Amp rejects common mode signals. Generally, CMRR is high (low CM gain) at low frequencies but drops -20 dB/decade as frequency increases. Thus, high frequency CM signals can be a problem. In this respect, the amplifier in Figure 3 will perform “better” than the amplifier in Figure 4.

This is an opportune point to digress into a discussion of “ground”. Clearly “voltage” must be measured between two points. “Ground” is the word used for the “reference” potential in a circuit and is generally assumed to be zero volts. Note however that Op Amps do not

have a ground terminal. Ground is implied. This is easy to ignore. After all, most amplifiers, at least the older ones, operate from $\pm 15\text{ V}$ or $\pm 12\text{ V}$ rails and are biased symmetrically above and below ground. “Ground” is than half way between the rails and everything works as long as your signals remain a volt or two inside the rails. However, what happens when you use a single supply Op Amp? If the amplifier in Figure 3 is operated from 5V to ground, caution is required because the non-inverting terminal is connected to ground. First, this will likely violate the common mode input range for the device because there is no “headroom” to bias the input circuitry properly⁷. Second, this is an inverting amplifier. However, as the output cannot go below ground, it will only work when V_i is negative. Finally, the amplifier will not work for small input voltages because the output cannot get close enough to ground to drive the inverting input to zero volts. Operating a single supply Op Amp in this manner is a very common error because there is a generally poor understanding of common mode input range.

There are a number of solutions to this problem and a great deal of literature on how to use single supply Op Amps. I will not present those solutions in detail here but generally they involve redefining “ground” by applying a reference voltage to the non-inverting terminal or by summing a fixed reference into the inverting input node. Caution must be used to prevent this reference from being amplified. One approach is to create a reference voltage at the midpoint of the supplies and redefine the circuit “grounds” to that voltage. This works well. The points are that “ground” is a concept that the designer has to address, there can be multiple “grounds” in a system, and keep in mind that Op Amps have a limited operating range that is bounded by (and likely inside) the supply rails.

Back to the ideal assumptions in Table 1; PSRR is power-supply rejection ratio and is similar to CMRR. The assumption is that variations on the power supply rails do not affect the output voltage, i.e. infinite PSRR. In fact, this is why Op Amps are frequently drawn without power pins. We generally assume that as long as the Op Amp has sufficient supply voltage to properly bias the internal circuitry, the power pins aren’t important. This is very dangerous as properly powering an Op Amp is critical to the performance of the amplifier. This is why power supply decoupling⁸ is necessary. In reality, the power pins are just another input and have to be engineered accordingly.

Finally, the general assumption is that the Op Amp is a noise free device. Noise is another topic that will not be addressed in detail at this point but I will touch on the basics⁹. Op Amps have three noise sources associated with them, a voltage noise source and a current noise source on each input. In fact, the noise model looks just like Figure 5 with V_{OS} replaced with e_n (the Op Amp voltage noise) and I_{bias+} and I_{bias-} replaced with i_{n-} and i_{n+} (the Op Amp current noise sources). The difference is that these are now AC sources. Again, the output contributions can be determined using superposition; however the analysis is more complex as these noise sources have a spectral density that is a function of frequency.

⁷ There are rail-to-rail Op Amps available, but read the datasheet carefully as rail-to-rail typically means operation within 50 mV (or more) of the supply rail. Also, a rail-to-rail output Op Amp is not necessarily a rail-to-rail input Op Amp, and visa versa. However, some rail-to-rail Op Amps can be operated in this manner provided V_i stays below zero volts.

⁸ Decoupling is a topic onto itself and will not be discussed in detail here. It involves using capacitors and possibly resistors or inductors to “decouple” the component from the power bus and prevent components from “talking” to each other over the power bus. Many datasheets do not show decoupling networks or only show minimal decoupling. That is because when a component is used by itself, little or no decoupling is needed. However, the manufacturers assume the designer will “engineer” the power distribution and grounding for a system and decoupling networks are implied.

⁹ A good starting point is “*Noise Analysis in Operational Amplifier Circuits*”, Texas Instruments, SLVA043A, 1999, “*Operational Amplifier Noise Prediction*”, Intersil, AN519.1, November 1996, and “*Noise Analysis Of FET Transimpedance Amplifiers*”, Texas Instruments, AB-076, 1994.

In addition, to get a true indication of the noise performance of an amplifier, the noise contributions from the resistors must be included. Resistors have a noise voltage given by

$$V_{nR} = \sqrt{4kTR\Delta f} \quad (11)$$

Where R is the value of the resistor, T is the temperature, k is Boltzmann's constant, and Δf is the noise bandwidth¹⁰. To properly analyze the noise performance of an Op Amp, it is necessary to know the details of the frequency response.

Now let's take a closer look at one of the key assumptions made above, infinite open loop gain. This assumption enabled us to quickly and easily analyze the circuits in Figures 3 and 4. Of course, the reality is that open loop gain is finite and is a function of frequency. Op Amp open loop gain is often approximated using a single pole at ~10Hz. Gains at DC can be 80 dB to 140 dB, depending on the speed or precision of the device, and a single pole causes a 90° phase shift. I'm jumping ahead a little, but problems don't occur until the phase shift¹¹ starts approaching 180°. Op Amps actually have several poles in their frequency response because internally they can have 2 to 5 amplifier stages. How much of an effect this has depends on the location of the other poles. A fully compensated Op Amp, also called unity-gain stable, is one in which the 2nd pole has been shifted up in frequency to the point where the phase shift is $\ll 180^\circ$ when $A_v = 0$ dB¹². This point is known as the unity-gain bandwidth or gain-bandwidth product (GBW or f_T).

Let's introduce some more definitions. The feedback factor (β) is defined as the fraction of the Op Amp output that is fed back to the input. This is a critical parameter and it will be shown below that much about the Op Amp's AC performance and stability can be predicted from this value. Using the amplifier from either Figure 3 or Figure 4 and removing the Op Amp for simplicity, the feedback factor can be defined as (reference Figure 6):

$$\beta = \frac{V_2}{V_1} = \frac{Z_i}{Z_i + Z_f} \quad (12)$$

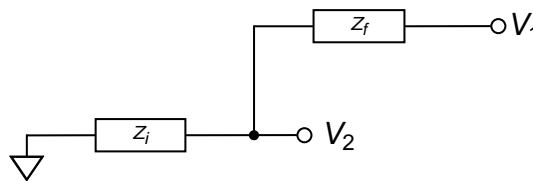


Figure 6: Op Amp Feedback Network

Next, we define the term “noise gain” as the reciprocal of β .

$$\text{Noise Gain} = \frac{1}{\beta} = \frac{Z_i + Z_f}{Z_i} = 1 + \frac{Z_f}{Z_i} \quad (13)$$

¹⁰ Equivalent Noise Bandwidth corresponds to a rectangular, or “brickwall” filter of bandwidth Δf with has the same noise power as the circuit bandwidth, i.e. the integrals over frequency are equal. For a single pole response typical in an Op Amp circuit, this is given by $\Delta f = f_{3dB}(\pi/2)$.

¹¹ Actually it is the phase shift associated with the loop gain A_{vl} that is important. $A_{vl} = A_v$ only when $Z_f = 0$ and $Z_i = \infty$. This will be discussed in more detail later.

¹² There may be a more formal definition out there but manufacturers vary a lot. As you will learn later, there are numerous effects that contribute to the phase and ultimately to stability of the amplifier. Many manufactures aim for a $<45^\circ$ phase margin for an Op Amp (difference between the phase at $A_v = 0$ dB and 180°). While this is a useful design consideration, it is not the complete story.

Finally, we define the loop gain, A_{vl} , as the gain around the feedback loop, as illustrated in Figure 7. The loop gain is given by

$$A_{vl} = \frac{V_0}{V_1} = \frac{Z_i}{Z_i + Z_f} A_v = A_v \beta \quad (14)$$

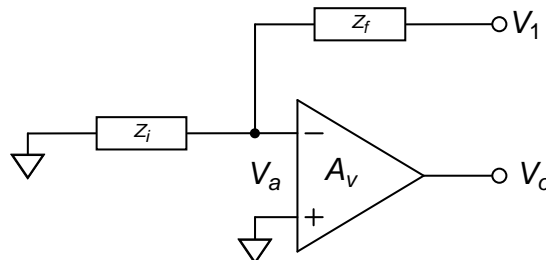


Figure 7: Op Amp Loop Gain

First, note that the noise gain is the same as the closed loop signal gain of a non-inverting amplifier configuration. Second, note that β and A_{vl} are the same regardless of which amplifier configuration, inverting or non-inverting, is examined. This is a good point to stop and reread this material because this is a critical observation. This means the performance of an amplifier circuit (stability, bandwidth, noise, overshoot, ringing, etc.) depend only on the open loop gain, A_v , and the feedback factor, β , and are otherwise independent of the amplifier configuration.

Returning to our discussion of open loop gain and bandwidth, the small signal bandwidth, or frequency response, or closed loop bandwidth¹³ of an amplifier is the frequency where the signal gain is 3 dB below the passband gain. It is a property of voltage feedback¹⁴ Op Amps that the closed loop bandwidth is given by f_T divided by the circuit noise gain, or $f_{CL} = f_T \beta$. Graphically, the above is summarized in the magnitude plot in Figure 8. Note that when plotted in dB, the difference between the open loop gain (A_v) and the noise gain is the loop gain ($A_v \beta$). This will be very useful later.

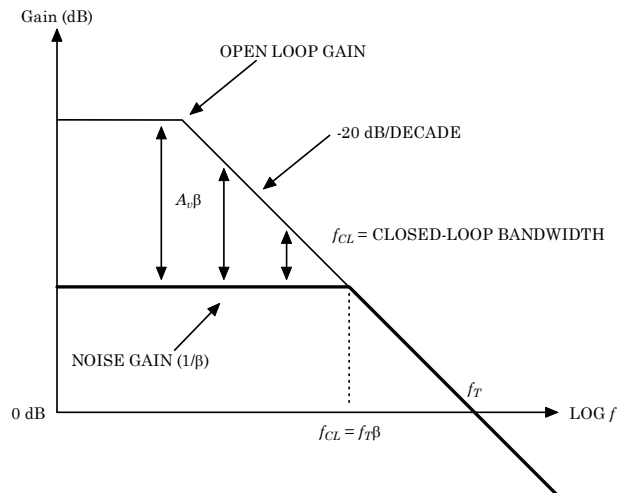


Figure 8: Op Amp Open Loop Gain and Noise Gain

¹³ Sorry to use so many terms but we engineers curse ourselves by frequently using numerous terms to describe the same characteristic or one term to describe multiple characteristics. Consider yourself warned.

¹⁴ Current feedback amplifiers do not follow the GBW relationship.

Now let's look closely at what happens if A_v is not infinite. Referring to the inverting amplifier in Figure 2 above, applying KCL at the inverting node, and noting that $V_o = \underline{A_v V_a}$, we can derive an expression for the closed loop inverting gain $A_{vcl}(inv)$.

$$\frac{V_i + V_a}{Z_i} + \frac{V_o + V_a}{Z_f} = 0 \quad (15)$$

$$\frac{V_i}{Z_i} + \frac{V_o}{A_v Z_i} + \frac{V_o}{Z_f} + \frac{V_o}{A_v Z_f} = 0 \quad (16)$$

$$V_o \left[\frac{1}{A_v Z_i} + \frac{1}{Z_f} + \frac{1}{A_v Z_f} \right] = -\frac{V_i}{Z_i} \quad (17)$$

$$\frac{V_o}{V_i} = A_{vcl}(inv) = -\frac{1}{Z_i} \frac{1}{\frac{1}{A_v Z_i} + \frac{1}{Z_f} + \frac{1}{A_v Z_f}} \quad (18)$$

$$A_{vcl}(inv) = -\frac{A_v Z_f}{Z_i + Z_f + A_v Z_i} \quad (19)$$

Which can be rewritten as:

$$A_{vcl}(inv) = -\frac{Z_f}{Z_i} \left(\frac{A_v}{\frac{Z_i + Z_f}{Z_i} + A_v} \right) \quad (20)$$

Recognizing that $\beta = \frac{Z_i}{Z_i + Z_f}$ and defining $\alpha = \frac{Z_f}{Z_i + Z_f}$, this equation can be simplified to:

$$A_{vcl}(inv) = -\frac{Z_f}{Z_i} \left(\frac{1}{1 + \frac{1}{A_v \beta}} \right) = -\frac{\alpha}{\beta} \left(\frac{1}{1 + \frac{1}{A_v \beta}} \right) \quad (21)$$

Note that as $A_v \rightarrow \infty$

$$A_{vcl}(inv) = -\frac{Z_f}{Z_i} = -\frac{\alpha}{\beta} \quad (22)$$

Similarly, for the non-inverting amplifier in Figure 3 we obtain an expression for the closed loop non-inverting gain $A_{vcl}(non)$.

$$A_{vcl}(non) = \left(1 + \frac{Z_f}{Z_i} \right) \left(\frac{1}{1 + \frac{1}{A_v \beta}} \right) = \frac{1}{\beta} \left(\frac{1}{1 + \frac{1}{A_v \beta}} \right) \quad (23)$$

Again as $A_v \rightarrow \infty$

$$A_{vcl}(non) = 1 + \frac{Z_f}{Z_i} = \frac{1}{\beta} \quad (24)$$

Notice that in both cases, the close loop gain is expressed as the ideal gain times an error term that is strictly a function of the loop gain $A_v\beta$. The gain error can be computed from:

$$Gain_Error = 1 - \frac{1}{1 + \frac{1}{A_v\beta}} \quad (25)$$

Note that:

$$\frac{1}{1 + \frac{1}{A_v\beta}} = \frac{A_v\beta}{1 + A_v\beta} \approx 1 - \frac{1}{A_v\beta} \quad (26)$$

Thus, the gain error can be simplified and expressed as a percentage using:

$$\varepsilon(\%) \approx \frac{100}{A_v\beta} \quad (27)$$

Figure 8 shows that $A_v\beta$ (shown graphically as the difference between the open loop gain and the noise gain) decreases with frequency. This is why high open loop gain is important and also why it is often necessary to select an Op Amp with high open loop gain and/or a higher than expected bandwidth. Otherwise the gain error given by Equation (27) can be large. Stability can also be impacted.

This brings us to the main topics of this discussion: feedback factor (β) and loop gain (A_{vl}). These terms are critical in assessing the AC performance and stability of any Op Amp configuration. Figures 9 and 10 show inverting and non-inverting amplifiers with signal gains of -2 and +2, respectively. For the inverting amplifier in Figure 9, $\beta = 1/3$ and for the non-inverting amplifier in Figure 10, $\beta = 1/2$. This corresponds to noise gains of 3 and 2, respectively.

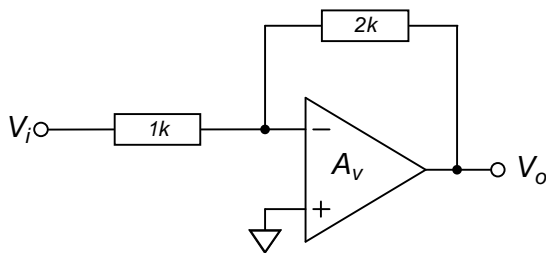


Figure 9. Inverting Gain of -2

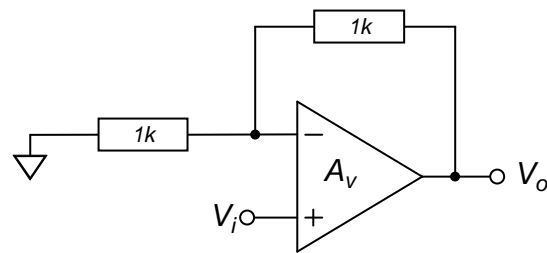


Figure 10. Non-Inverting Gain of +2

This means that while these amplifiers have the same signal gain¹⁵, the non-inverting amplifier has a higher bandwidth because it has a lower noise gain! Remember, bandwidth is given by $fT\beta$.

¹⁵ Yes, I'm ignoring the minus sign. In a great many cases a 180° phase shift can be ignored.

Another brief aside, using the terminology presented above, we can represent the inverting and non-inverting as control system blocks as shown in Figures 11 and 12. This notation is commonly used in a number of texts.

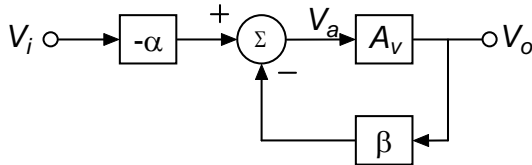


Figure 11. Inverting Amplifier Block Diagram

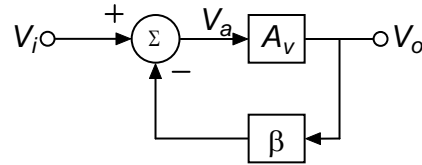


Figure 12. Non-Inverting Amplifier Block Diagram

Now we can finally start discussing stability. The Nyquist Criterion states that a circuit will oscillate if the loop gain $A_v\beta = 1 \angle 180^\circ$. From the discussion above, we already know that A_v contributes at least a 90° phase shift and in many cases we may not have much leeway to select a different amplifier. So the stability of the amplifier will depend largely on the characteristics of β . However, it is not sufficient just to insure that the phase of the loop gain is less than 180° . Yes, the amplifier might not spontaneously oscillate, but as $A_v\beta$ approaches 180° , the amplifier will exhibit increasing overshoot and ringing in its step response. Generally, 135° , or a phase margin of 45° , is a good starting point. However, more phase margin may be required, or a lower phase margin may have to be tolerated, depending on the individual application.

But wait a minute. If you are using an Op Amp with purely resistive feedback, β doesn't contribute a phase shift. So provided the open-loop gain doesn't introduce an excessive phase shift, everything works, right? Wrong. As with most things, it is what you don't see that will ruin your day.

There are a number of "components" missing from the circuits in Figures 3 and 4. Above we alluded to a "source resistance", a characteristic of whatever is driving the input of the amplifier. In reality this is an impedance which can change the loop gain. The amplifier also drives a load, so load impedance has to be considered. A real Op Amp has a finite output impedance which interacts with the load to alter the loop gain. An Op Amp also has differential and common mode input impedances (typically modeled as high value resistors in parallel with a small capacitance). These also affect the loop gain. Finally, every circuit has stray capacitances that are a function of the circuit construction methodology. These can be minimized but not eliminated.

At this point the simple Op Amp circuits we discussed above are getting pretty ugly. As a general rule, if you have a high source impedance, a large capacitive load, large feedback resistors, or want a high frequency response, you need to take a close look at the loop gain¹⁶. You can analyze the circuit by hand or use one of the many graphical shortcuts to determine the loop gain, but this is time consuming (and can be quite intimidating even though you really only need the loop gain at a single frequency). You can build the circuit and try and measure the loop gain, but I am not a big fan of iterative design. The alternative I use is to simulate the amplifier using PSpice or some other circuit simulation package.

Circuit simulation software is dangerous. There is a significant tendency to blindly rely on what the computer predicts without having a good understanding of the circuit or the models

¹⁶ This comes down to the question "how big is big?" Unfortunately too many things are interrelated to give set guidelines. You will have to develop your own experience.

being used. A cute example is the uA771. Odds are that the macromodel in your software package includes a value of $R_p = 10.00E-3$. R_p is the power dissipation resistance and is only used to simulate the current drawn from the power supply. Assuming supply rails of $\pm 15V$, this model will draw 90 kW. Obviously this is a typographic error and it should probably be $10.00E3$. The point is that macromodels can contain errors and, more importantly, only model a limited set of parameters for a given amplifier. Sometimes they are quite basic and leave out PSRR, CMRR, input and output impedances, etc. Be very skeptical of any model and study the macromodel to learn its limitations.

Obtaining the open loop gain from a simulation is problematic. Simply connecting the Op Amp in an open loop configuration will likely yield erroneous results, especially with newer macromodels. This is because as manufacturers have improved their macromodels, for example by adding additional structures to the inputs to more accurately simulate bias current compensation, it is important that the inputs be properly biased in order to correctly simulate the AC response of the Op Amp. With that said, there is a very good application note¹⁷ from Harris Semiconductor that gives a reliable method for obtaining open loop gain, loop gain, and feedback factor for a given amplifier configuration. This is shown in Figure 13. R_1 and R_2 provide a DC bias for the Op Amp input. However, C_1 effectively shorts the inverting input to ground for AC signals. Thus, at DC the Op Amp is properly biased and for AC R_2 appears as a negligible load on the output. So the probes on U1 pin 6 give the magnitude (in dB) and phase of A_v directly (because our input signal is 1V).

Now that we have A_v , we need to obtain the feedback factor, β . In Figure 13 below, R_f is the feedback resistor and R_i the input resistor. The divider formed by R_f and R_i represents the feedback factor β . The point where these two resistors connect yields $A_v\beta$. Because the markers are in dB, the difference between the markers is the noise gain, $1/\beta$ (in dB). With 1k and 10k resistor values, the noise gain is 11.

I added components¹⁸ to the schematic to model input capacitance, C_{in} , load capacitance, C_{load} , and feedback capacitance, C_f . You can easily add other components to introduce stray impedances or source impedances if required. Using this approach, you can fairly accurately determine the phase margin for your design. You should still study the Op Amp macro model to fully understand the limits of your simulation.

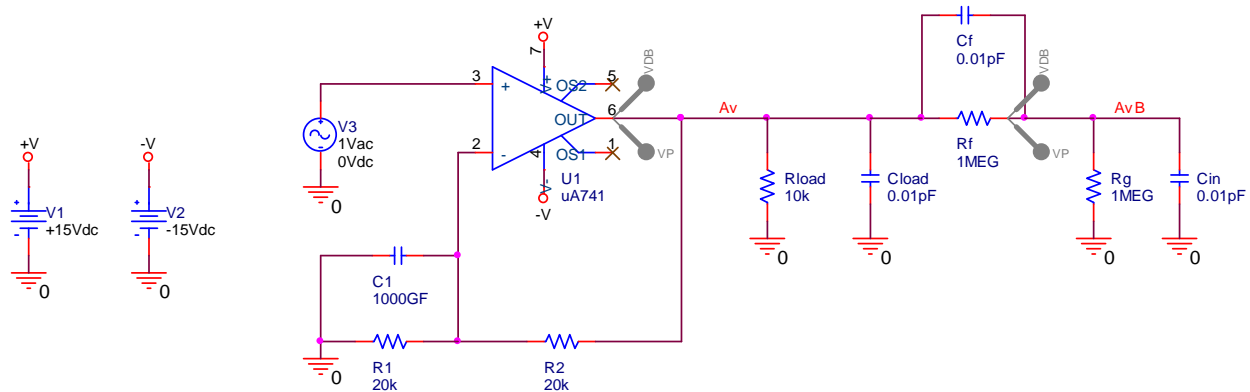


Figure 13. Open Loop Gain Simulation

¹⁷ "PSPICE Performs Open Loop Stability Analysis (HA5112)", Harris Semiconductor, November, 1996, AN9536.1.

¹⁸ I leave these components in my simulation even if they are not required as a value of 0.01pF is so small as to not matter.

Using this model, we can now take a quick look at some apparently minor but in reality significant issues. First, let's simulate the circuit using $R_f = R_i = 1\text{ k}\Omega$, $C_i = 20\text{ pF}$, and leave $C_{load} = C_f = 0.01\text{ pF}$. Then let's change $R_f = R_i = 1\text{ M}\Omega$ leaving the other values unchanged. The results are shown in Figures 14 and 15 below.

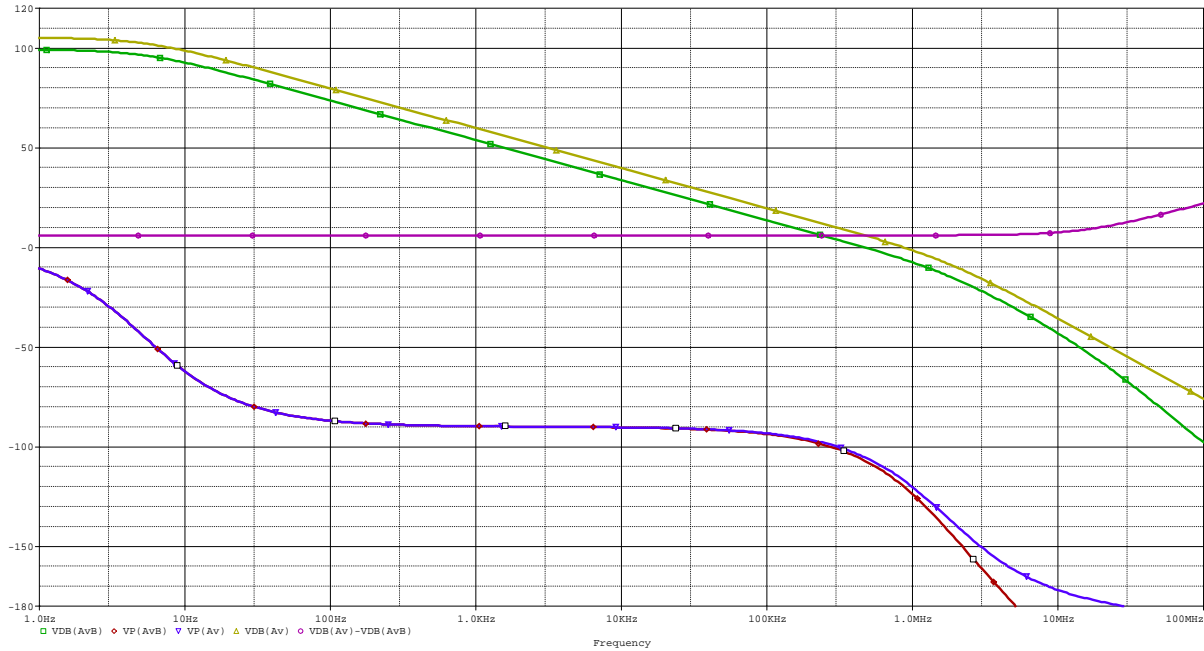


Figure 14. μA741 frequency response, gain of 2, $1\text{ k}\Omega$

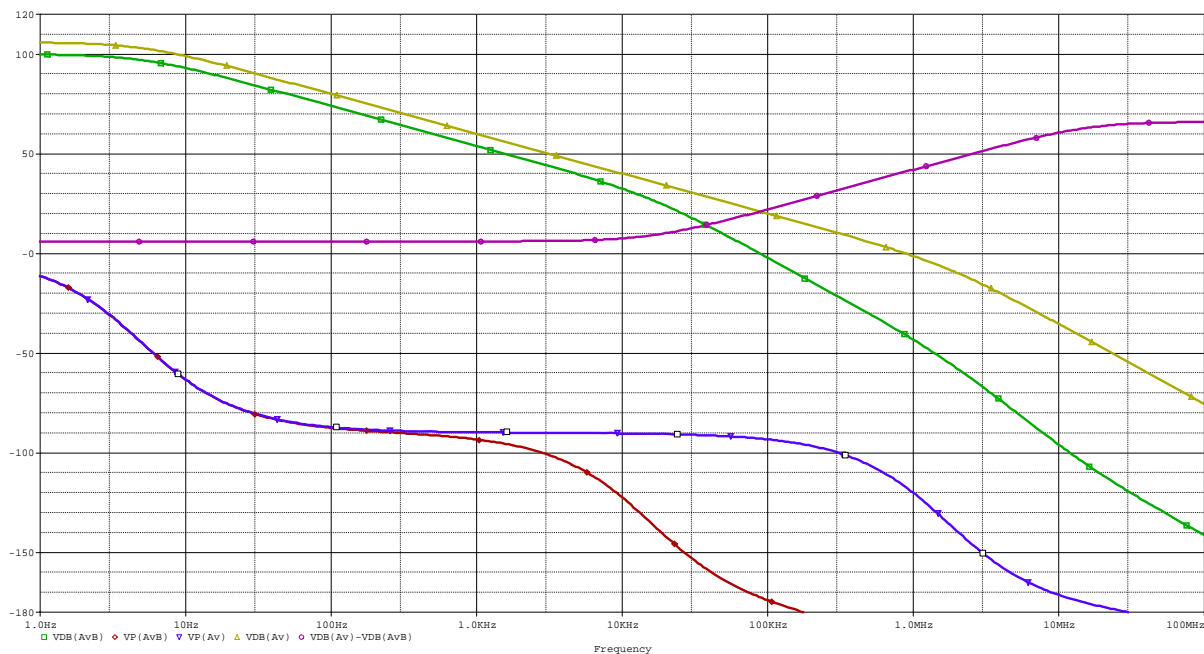


Figure 15. μA741 frequency response, gain of 2, $1\text{ M}\Omega$

The open loop gain (yellow) and phase (blue) are the same, as expected. However the loop gain (green) and phase (red), and noise gain (magenta) change significantly. With the $1\text{ k}\Omega$

resistors, the phase margin is $\sim 70^\circ$. With the $1\text{ M}\Omega$ resistors, the phase margin has dropped to less than 10° . As it turns out, 20 pF is a very reasonable value for the input capacitance (differential plus common mode) of an Op Amp. If you construct your circuit on a white prototyping board, the stray capacitance introduced can be much higher.

Figures 16 and 17 show the effect on the step response of the amplifiers. With a phase margin near 70° , the step response is well behaved. However, as the phase margin nears 180° , ringing dominates the response (although the oscillation is not sustained).

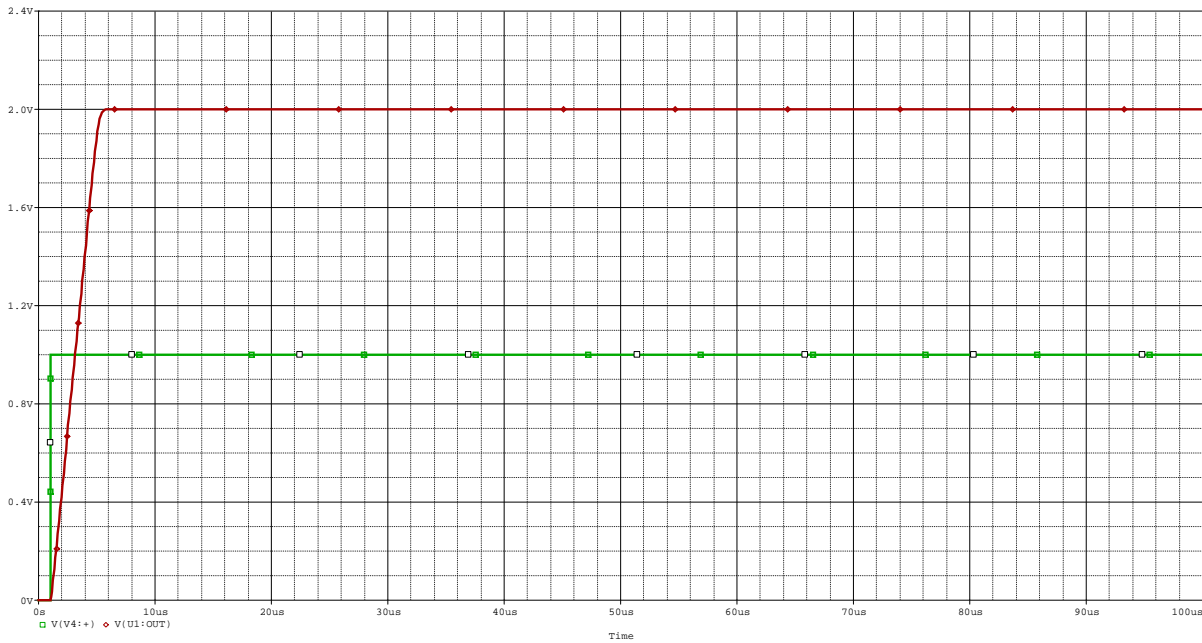


Figure 16. μA741 transient response, gain of 2, $1\text{ k}\Omega$

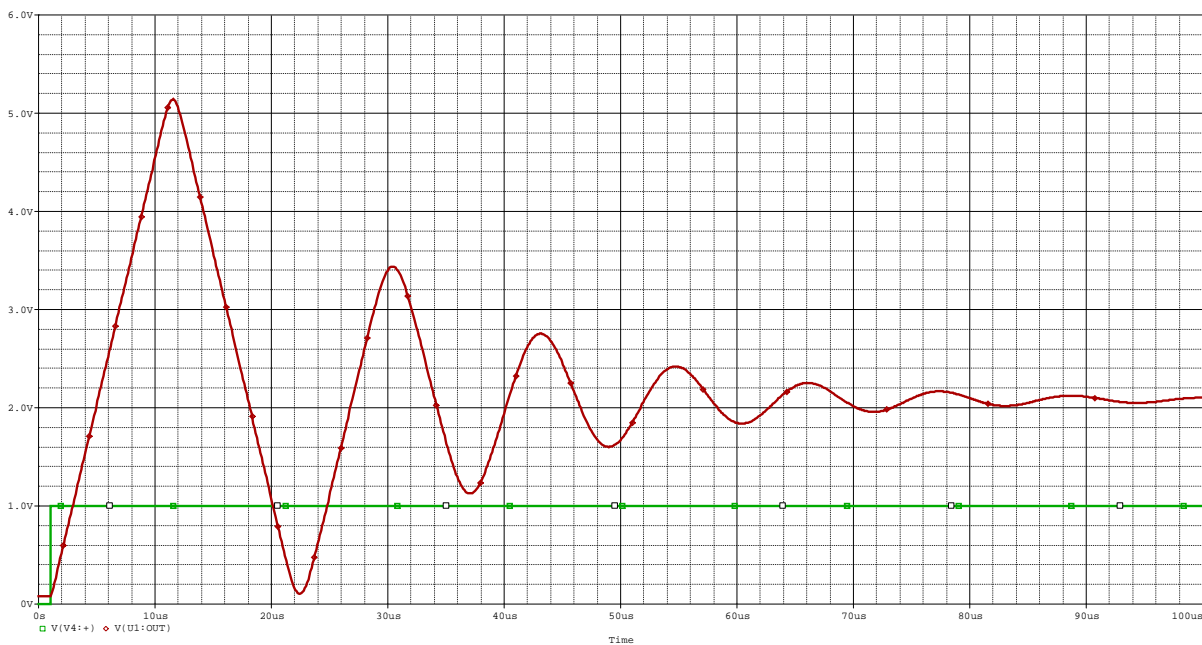


Figure 17. μA741 transient response, gain of 2, $1\text{ M}\Omega$

Refer back to Figures 14 and 15 and note the amplitude responses. For the 1 k Ω resistors, the noise gain is flat out to the intersection with the open loop gain. With the 1 M Ω resistors, there is a significant peak in the noise gain¹⁹ (~20 dB for this case). Recall that the closed loop bandwidth is $f_{CL} = f_T\beta$. What is the closed loop bandwidth when there is a peak in the noise gain? By this strict definition, the bandwidth of the 1 M Ω amplifier is ~100 kHz, 5 times less than the amplifier built using the 1 k Ω resistors. This is true even though both amplifiers have the same noise gain at 500 kHz. This makes sense if you think in terms of “when does the amplifier stop being an amplifier?” The answer is that the loop gain is equal to or less than 0 dB. Think of it this way: when the loop gain is < 0 dB the amplifier can no longer drive the input differential voltage to zero (a key assumption from above). Therefore, at this point all semblance of ideal behavior is gone.

There is one additional effect that is worth illustrating before moving to a discussion of poles and zeros. Figure 18 repeats the AC simulation using $R_f = R_i = 1$ M Ω , $C_i = 20$ pF, but this time includes $C_f = 5$ pF. Compare this to Figure 15 and notice that we now have a phase margin of nearly 80°, ~2.5 times the bandwidth, and > 6 db reduction in peaking. This illustrates why Bob Pease²⁰ states that you always include a small feedback capacitor “unless you can prove you don’t need it”.

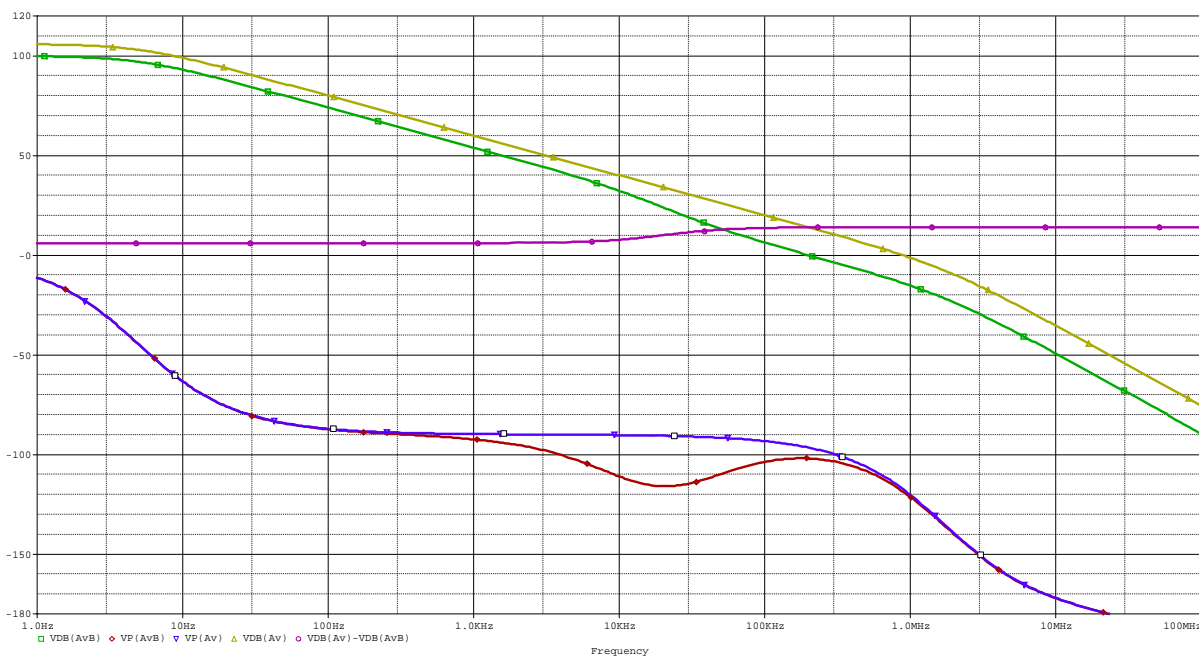


Figure 18. μ A741 frequency response, gain of 2, 1 M Ω with $C_f = 5$ pF

Let’s move on to poles and zeros. I’ve repeated the simulation above but I increased C_i to 200 pF to separate the poles from the zero in the loop gain. Recall that a pole (zero) causes a -90° (90°) phase shift with the pole (zero) located at -45° (45°). Looking at the phase of the loop gain (red trace) in Figure 19, it can be seen that there are poles at 5 Hz (pole #1), 1.7 kHz (pole #2), and 1.6 MHz (pole #3) and a zero at 30 kHz (zero #1). Poles #1 and #3 are

¹⁹ Note that the noise gain does not continue to increase beyond the open loop gain. Once the loop gain is zero, there is no longer any feedback. Beyond this point the noise gain is equal to the open loop gain.

²⁰ Bob Pease is an analog guru at National Semiconductor. Bob has many good books, webcasts, and magazine articles that I highly recommend you pursue.

due to the open loop gain and are seen in the yellow trace. Pole #2 and zero #1 are caused by the feedback network²¹ and the locations are given by

$$f_{P2} = \frac{1}{2\pi(R_f \parallel R_i)(C_f \parallel C_i)} \quad (28)$$

$$f_{Z1} = \frac{1}{2\pi R_f C_f} \quad (29)$$

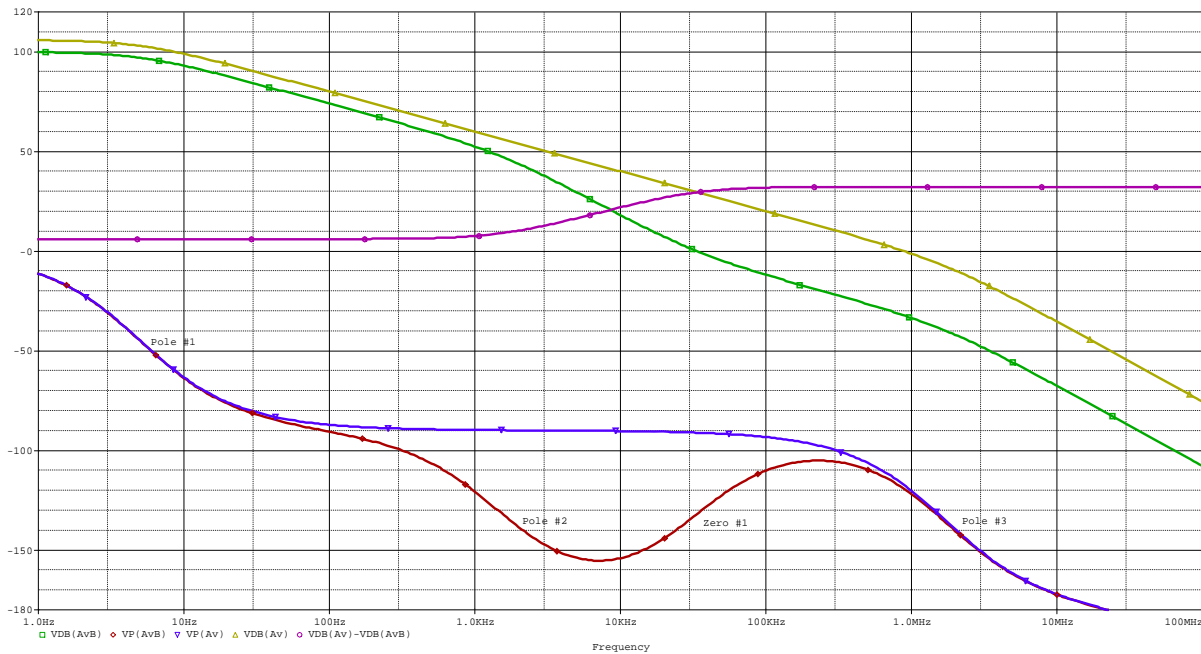


Figure 19. $\mu A741$ frequency response, gain of 2, $1\text{ M}\Omega$ with $C_f = 5\text{ pF}$, $C_{in} = 200\text{ pF}$

Because the noise gain is given by the reciprocal of β , it is the pole in the loop gain that causes the peaking in the noise gain and the zero in the loop gain that reduces this peak. Looking at Equations (28) and (29) you can see that in all cases, $f_{Z1} \geq f_{P2}$. As it turns out, the maximum value of the peak is given by $(1 + C_i/C_f)$ (32 dB in Figure 19).

Looking at Equations (28) and (29), when R_f , R_i , C_f and C_i are small, the pole and zero in the loop gain are at (relatively) high frequencies and don't matter. It is only when we 1) need more bandwidth and switch to a higher frequency Op Amp such that the open loop gain extends out to encompass f_{p2} , 2) are forced to use high value resistors in the circuit (e.g. when interfacing to high impedance sensors such as photodiodes), 3) have a board layout with lots of stray capacitance, and/or 4) have to drive a large capacitive load²². The technique applied above permits a rapid and flexible means of analyzing all of these cases provided the design engineer is familiar with the circuit, application, and models used.

There are a few more notes to make about the frequency response plots above. The noise gain is shown to extend out to very high frequencies. In reality this is not the case as it

²¹ Note that we are focusing on the feedback and input resistors and capacitors for this discussion. Keep in mind however that the Op Amp output impedance, load impedance, source impedance, and strays could all have an impact on the frequency response and stability. I'm just trying to keep the discussion simple.

²² A capacitive load combines with the Op Amp output impedance to create a pole in the loop gain which can decrease the phase margin. Note that output impedance may not be modeled correctly so don't assume anything.

does roll off with the open loop gain (although feedback factor does not for obvious reasons). Accounting for this rolloff is important when performing a noise analysis as otherwise the noise integral would be infinite. A more accurate representation of the noise gain can be obtained by including the error term discussed above (see Equation (23)). This typically is not included in a stability analysis because the angle created by the intersection of the open loop gain curve and $1/\beta$ can be used to assess the stability of the amplifier. If the difference between the slope of the noise gain and the slope of the open loop gain where they intersect is less than zero, the system is stable.

For example, in Figure 14 the noise gain has a slope of zero when it intersects the open loop gain, which has a slope of -20 dB/decade. Thus the difference is -20 dB/decade and the system is stable (as reflected by the large phase margin). However, in Figure 15 the noise gain has a slope nearly equal to $+20$ dB/decade at the intersection, so the difference is only slightly less than 0 dB/decade. While still stable, the amplifier has considerable ringing and a very low phase margin. Note that the locations of the poles in the open loop gain can be obtained from the data sheet for the Op Amp and the locations of the poles and zeros in the noise gain can be obtained by a simple circuit analysis (this is how I came up with Equations (28) and (29)). Thus, without using PSpice, asymptotic plots of the magnitude response can be drawn and, while not completely precise, they will reveal potential problems *without having to compute the phase response*. I like that. More importantly, it is pretty easy to remember Equations (28) and (29) such that, with a little experience, you can almost do the analysis in your head. Note that I have neglected to include the effect of output impedance and load capacitance. This adds another pole to the feedback factor (a zero in the noise gain – bad news!). This can be ignored if the load capacitance is low (but watch high frequency applications...Op Amp output impedance is not constant with frequency.

In the discussions above, β , noise gain, bandwidth, stability, are all small signal characteristics of an Op Amp. They matter even if you are not planning on using the Op Amp for AC signals as the noise inherent in the Op Amp is sufficient to initiate oscillation. However, Op Amps are frequently used to produce signals that do not meet the small signal criteria²³. The point of understanding small signal amplitude is to know the point at which the output may start being distorted by large signal characteristics such as output drive capability or slew rate limiting.

Output drive is straightforward; there is a limit to how much current an Op Amp output can source (sink). Most of the specifications in the datasheet are based on the Op Amp driving a load of a few $k\Omega$ ²⁴. Problems can arise when the output has a significant capacitive component as the impedance of the capacitor in parallel with the resistive load may reduce the load impedance to the point where the output drive capability of the Op Amp is exceeded.

²³ This is the question of how small is small? Usually the manufacturer's data sheet will give you some information as to the conditions under which small signal specifications are tested. An output signal amplitude of $1V$ is not uncommon, although some amplifiers are specified for outputs of $100mV$. You need to always read the entire datasheet and sometimes you need to use your best judgment.

²⁴ As an aside it is important to note that certain analog components (e.g. analog multipliers) require a fairly specific load resistance for accurate operation. Others just need a load that is neither too small (requiring a high current) or too large (poles introduced by strays as discussed above). For Op Amps, loads of $1k\Omega$ to $100k\Omega$ are generally safe.

In the discussion of ideal characteristics at the beginning of this document it is stated that slew rate is a large signal parameter and a measure of how fast the output voltage of an Op Amp change. Put another way, the slew rate for the Op Amp must be greater than the maximum slope of the output waveform over the range of frequencies being examined. If this condition is met, the response will be determined by the bandwidth and not by slew rate limiting.

Start to think about it this way. For small signal operation, the output is limited by the small signal bandwidth of the Op Amp. As the output signal amplitude increases, at some point the Op Amp will transition to where large signal parameters like slew rate begin to dominate. Take the output sine wave

$$v_o(t) = V_{peak} \sin(2\pi ft) \quad (30)$$

The maximum slew rate for this signal is given at the zero crossing, or:

$$\left. \frac{dv_o(t)}{dt} \right|_{MAX} = 2\pi f V_{peak} \quad (31)$$

Thus, the slew rate required for an undistorted output is a function of the output amplitude and the frequency of the signal. Thus, the minimum²⁵ slew rate specification for the Op Amp must meet the following criteria to avoid slew rate limiting:

$$SR_{min} > 2\pi f V_{peak} \quad (32)$$

There is a special case where we set the maximum slew rate of the output sinusoid equal to the specified slew rate of the Op Amp. This is called the full-power bandwidth. It is a large signal parameter and is defined at the highest frequency “full-amplitude” sinusoid that can be output without slew rate distortion. Again, “full-amplitude” is a relative term. Usually a 20 V_{PP} sinusoid is used. This was because you typically could not get closer than about two diode drops to the rail and it worked for both ±15 V and ±12 V supplies, which were common. However, now with rails at 5V or 3.3V or less, the definition has to adapt. Again, use your judgment and read the manufacturer’s data sheet to determine how they test this specification. Adjusting the equation above,

$$f_{FPBW} = \frac{SR}{2\pi V_{peak}} \quad (33)$$

If you exceed the frequency given by the equation above, the output sine wave will quickly become a triangle wave.

So far we have been discussing the effect of these small- and large-signal parameters on sinusoidal signals. For square wave outputs, slew rate limiting and bandwidth can both affect the output waveform. Keep in mind that a square wave has essentially an infinite slope. In reality, the input square wave has a slope much larger than what can be represented at the output of the amplifier. What you will get out depends on which specification dominates; bandwidth limiting or slew rate limiting.

²⁵ Use caution when looking at specifications in the data sheet. “Typical” means just that. It is not a guarantee and minimum or maximum specifications should be used to insure your design operates properly under all conditions.

First, look at the step response due to the bandwidth. Recall that the bandwidth causes a single pole in frequency response of the amplifier. The pole is at

$$\omega_o = 2\pi f_T \beta \quad (34)$$

where $1/\beta$ is the amplifier noise gain and f_T is the gain-bandwidth product. The response of a first-order system to a step (square wave) is:

$$V_o(s) = \frac{\omega_o V_{\max}}{s(s + \omega_o)} \quad (35)$$

This results in an exponential response of the form:

$$v_o(t) = V_{\max} (1 - e^{-\omega_o t}) \quad (36)$$

The output will look like an exponential with an initial slope of

$$\left. \frac{dv_o}{dt} \right|_{MAX} = V_{\max} \omega_o = V_{\max} 2\pi f_T \beta \quad (37)$$

If the Op Amp slew rate is greater than this value, the exponential response will be preserved and bandwidth limiting dominates. This is usually the case when V_{\max} is small or $1/\beta$ is large.

If you instead want to measure the slew rate of the Op Amp, you would use a small gain (typically unity) with a large voltage step (like 10 V) big enough to cause the Op Amp slew rate specification to be much SMALLER than this slope. The result will be a linear ramp with slope equal to the Op Amp slew rate. Keep in mind that in one case, we are still looking at a small signal response (exponential response due to bandwidth limiting) and in the other, a large signal parameter (slew rate limiting).

Before I wrap-up, this is a good point for an aside about making measurements on Op Amp circuits. First, from the discussion on stability above, I hope it is clear that probing the node connected to the inverting input is nearly pointless. Connecting a scope probe or DMM lead to this input adds considerable capacitance and alters the noise gain, making any signal at the output of the Op Amp meaningless. I say “nearly” because there is one thing that can be learned by measuring the voltages at the inverting and non-inverting inputs. If the Op Amp has the proper supply voltages and the voltage difference between these nodes is not zero, the Op Amp is not functioning properly. Often the culprit is a bad connection in the feedback loop, but there can be other causes as well.

While sinusoids are great test signals, they are not all inclusive. Always apply an input step or square wave to your circuit and look at the rise time of the exponential and the slew rate as discussed as above. This will also reveal any possible stability issues (in the form of ringing) in your amplifier configuration.

The rise time of the exponential can provide considerable insight into your circuit provided you are careful in setting up the measurement. Rise time is defined as the time it takes for a signal to rise (or fall for fall time) from 10% to 90% of its final value. There is a clearly defined relationship between the rise time and the bandwidth of an amplifier. However, you need to use caution to be certain you are measuring the performance of your circuit and not the limitations of your test equipment.

The relationship between rise time and small-signal bandwidth is given by:

$$t_{rise} = \frac{0.35}{f_{3dB}} \quad (38)$$

Recognizing that for a simple RC circuit $f_{3dB} = (2\pi RC)^{-1}$, this is equivalent to:

$$t_{rise} = 2.2RC \quad (39)$$

These equations should be committed to memory, as it is extremely useful in both design and debugging. These equations assume the signal is being affected by a single dominant pole in the transfer function, as is typically the case in Op Amp circuits. However, in the case where the signal passes through cascaded transfer functions (such as an amplifier chain or an amplifier under test, scope probe, and scope amplifier), the overall rise time can be approximated by:

$$t_{rise} \approx 1.1\sqrt{t_{rise_1}^2 + t_{rise_2}^2 + \dots + t_{rise_n}^2} \quad (40)$$

More commonly, the bandwidths of the individual transfer functions are known, or Equation (40) can be rewritten as²⁶:

$$f_{3dB} \approx \frac{1}{1.1\sqrt{f_{3dB_1}^{-2} + f_{3dB_2}^{-2} + \dots + f_{3dB_n}^{-2}}} \quad (41)$$

Equation (38) can be derived as follows. Start with the transfer function for a single pole system, $H(s)$.

$$H(s) = \frac{k}{s + \omega_0} \quad (42)$$

Given that the input is a step function:

$$v_i(t) = u(t) \quad (43)$$

$$V_i(s) = \frac{1}{s} \quad (44)$$

Therefore:

$$V_o(s) = \frac{k}{s(s + \omega_0)} \quad (45)$$

Applying partial fraction expansion

$$\frac{k}{s(s + \omega_0)} = \frac{A}{s} + \frac{B}{s + \omega_0} \quad (46)$$

$$A = \left. \frac{k}{s + \omega_0} \right|_{s=0} = \frac{k}{\omega_0} = k_0 \quad (47)$$

²⁶ Note that some references leave out the factor of 1.1 but for most applications it improves the agreement between the approximation and reality.

$$B = \frac{k}{s} \Big|_{s=-\tau^{-1}} = -\frac{k}{\omega_0} = -k_0 \quad (48)$$

$$\frac{k}{s(s + \omega_0)} = \frac{k_0}{s} - \frac{k_0}{s + \omega_0} \quad (49)$$

Taking the inverse Laplace transform yields:

$$v_0(t) = k_0(1 - e^{-at}) \quad (50)$$

Rise time is defined as:

$$t_r = t_{0.9} - t_{0.1} \quad (51)$$

Where

$t_{0.9}$ = time at which $v_0(t)$ reaches 90% of its steady state value

$t_{0.1}$ = time at which $v_0(t)$ reaches 10% of its steady state value

Using Equation (50)

$$v_0(t_{0.9}) = 0.9k_0 = k_0(1 - e^{-\omega_0 t_{0.9}}) \quad (52)$$

$$0.9 = 1 - e^{-\omega_0 t_{0.9}} \quad (53)$$

$$-\omega_0 t_{0.9} = \ln 0.1 \quad (54)$$

$$t_{0.9} = -\frac{\ln 0.1}{\omega_0} \quad (55)$$

$$v_0(t_{0.1}) = 0.1k_0 = k_0(1 - e^{-\omega_0 t_{0.1}}) \quad (56)$$

$$t_{0.1} = -\frac{\ln 0.9}{\omega_0} \quad (57)$$

$$t_r = t_{0.9} - t_{0.1} = -\frac{\ln 0.1}{\omega_0} + \frac{\ln 0.9}{\omega_0} \quad (58)$$

$$t_r = \frac{1}{\omega_0} (\ln 10 - \ln \frac{10}{9}) \quad (59)$$

Note that $\omega_0 = 2\pi f_{3dB}$. Substituting yields

$$t_r = \frac{\ln 10 - \ln \frac{10}{9}}{2\pi} \left(\frac{1}{f_{3dB}} \right) \quad (60)$$

or

$$t_r = \frac{0.35}{f_{3dB}} \quad (61)$$

The approximations in Equations (40) and (41) can be verified using the Laplace modeling block in PSpice.

So what is the point of Equations (38), (39), (40), or (41)? One very useful application comes in when using an oscilloscope. Let's assume we want to look at the clock in a digital system. Do we care if it is a 1 MHz clock, 10 MHz clock, or 100 MHz clock? In reality, the frequency of the clock is unimportant. What matters is the rise time! Modern logic families have rise times on the order of 1 ns. Using Equation (38) this corresponds to a signal bandwidth of

$$f_{3dB} = \frac{0.35}{1ns} = 350MHz \quad (63)$$

When viewed on the scope display, the rise time observed will be a combination of the rise times of the signals being measured, the oscilloscope probe, and the oscilloscope preamp, as given by:

$$t_{rise} \approx 1.1\sqrt{t_{rise}^2(Scope_Amplifier) + t_{rise}^2(Scope_Probe) + t_{rise}^2(Signal)^2} \quad (62)$$

Assume that a 500 MHz oscilloscope and a 500 MHz probe are available for making this measurement. The rise time observed will be closer to 1.55 ns, a ~50% error. For this reason, it is very useful to compute the best-case rise time for the scope/probe combination you are using and keep this in mind as you are making measurements. *If the apparent rise time of the signal you are viewing approaches the best-case value, your scope is limiting the measurement and there may be features in the signal that are hidden from you.*

The material above may seem a little overwhelming the first time you read it. No doubt your brain glazed over a few times. This document was not intended to answer all of your questions or address all of the conditions where Op Amps can misbehave. The intention is to plant some seeds and illustrate the techniques for insuring that an Op Amp circuit will function properly, or conversely, to show you where to look if a circuit isn't working as expected. Now you need to start playing with the simulations and, most important, building circuits.

Addendum

As is usually the case, thoughts come to you after you think you have completed a task. Rather than continue to revise the material above, I have decided to add notes below to cover additional pointers for using Op Amps. Eventually this material will be incorporated into the discussions above.

1. **Bias Currents:** Another common error is to neglect to provide a DC path for the input bias currents. For example, if you AC couple the input to a non-inverting amplifier, you must place a resistor to ground from the non-inverting input or the bias current will charge the coupling capacitor. The result is that after a time, the output of the amplifier will saturate. This usually is not a problem with the inverting input as it is either DC coupled to the output, or in the case of an integrator, DC coupled to the input. However, I have seen designers combine integration and differentiation functions in a single amplifier. Be sure to provide a DC path (most likely to ground). The drawback in all cases is that adding a bias resistor can add noise to the circuit in the form of the thermal noise of the resistor and the voltage developed by that inputs' noise current. Everything has its price!

2. **Output Impedance** – It is not always safe to assume that the output impedance of an Op Amp is low. As the amplifier's open loop gain decreases, its closed loop output impedance increases. This can cause interesting effects when the Op Amp is configured as an inverting amplifier because there is a direct signal path from the input to the output (often a DC path). There is a particular issue with Sallen-Key (aka VCVS) active filter configurations. For example, in a low pass filter using this configuration, the response will roll off as expected and then actually rise until the open loop gain reaches 0 dB. At this point the response flattens out. Not what one expects from a low pass filter. When selecting an amplifier for a Sallen-Key filter, pay close attention to the output impedance and open loop gain as you can minimize (but not eliminate) this problem. Most designers put a passive RC filter on the output but use caution as this can adversely affect the phase response of the amplifier. While there are other active filter topologies, the Sallen-Key configuration is popular as it lends itself to single supply design because it is non-inverting.