Operational Amplifiers: Part 2

Non-ideal Behavior of Feedback Amplifiers
DC Errors and Large-Signal Operation

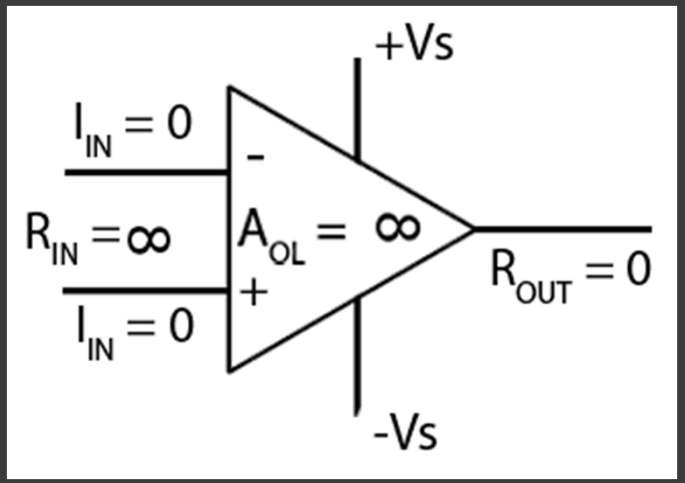
by

Tim J. Sobering

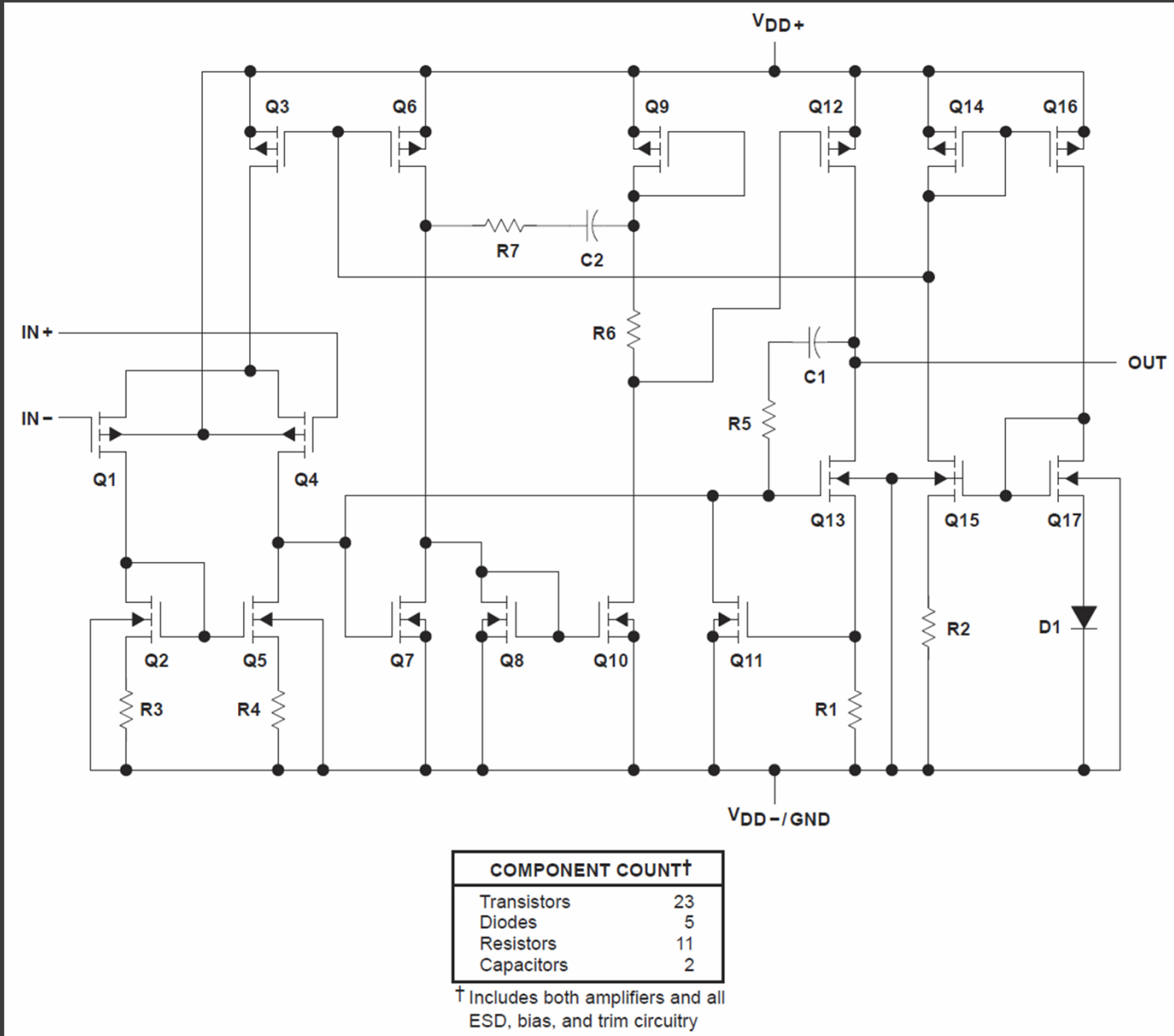
Analog Design Engineer
& Op Amp Addict

Summary of Ideal Op Amp Assumptions

- Zero input offset voltage (V_{os})
- Zero input bias current (I_{Bias}^{+}, I_{Bias}^{-})
- Infinite slew rate
  - Infinite large-signal (or full-power) bandwidth
- Infinite output drive
- No voltage rail limits
- Zero output impedance (Z_o)
- Infinite input impedance (Z_i)
- Infinite small-signal bandwidth
- Infinite open-loop gain (A_v)
  - Actually, infinite gain for a differential input, zero gain for a common mode input



Op Amp Internals – TLV2721C (just for fun)

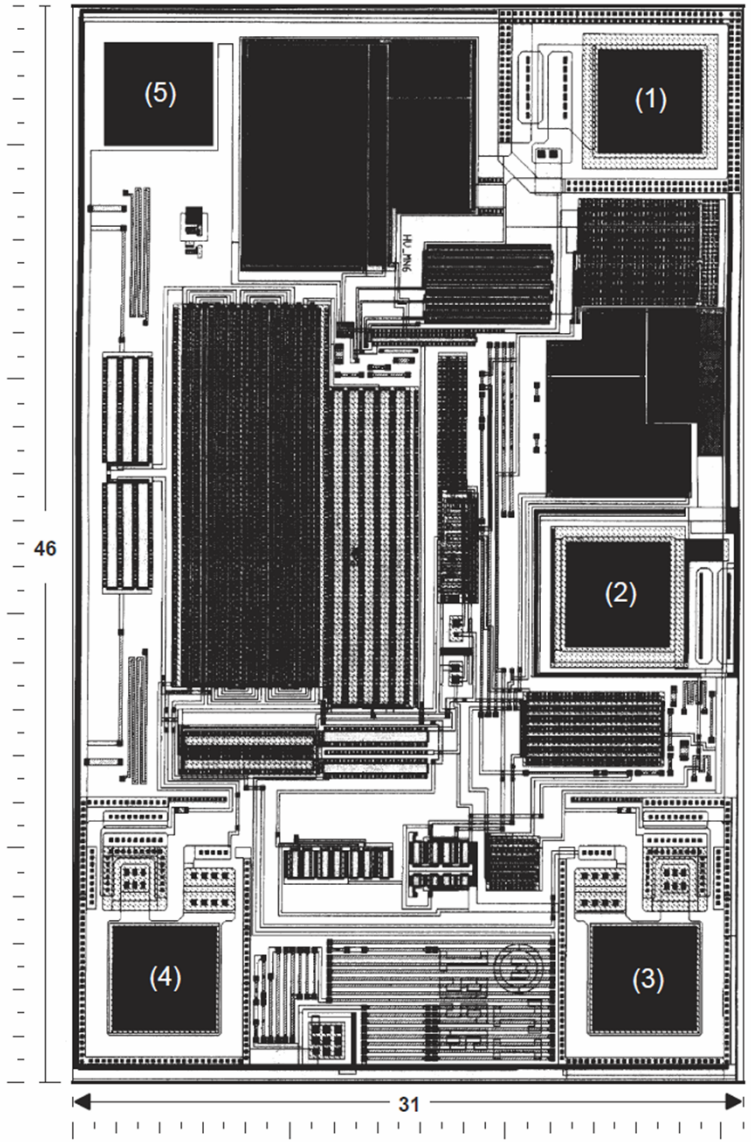


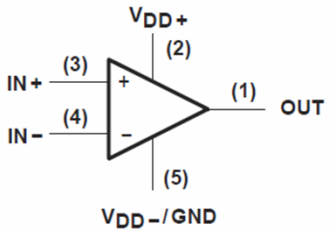
COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

Op Amp Internals – TLV2721C (just for fun)

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

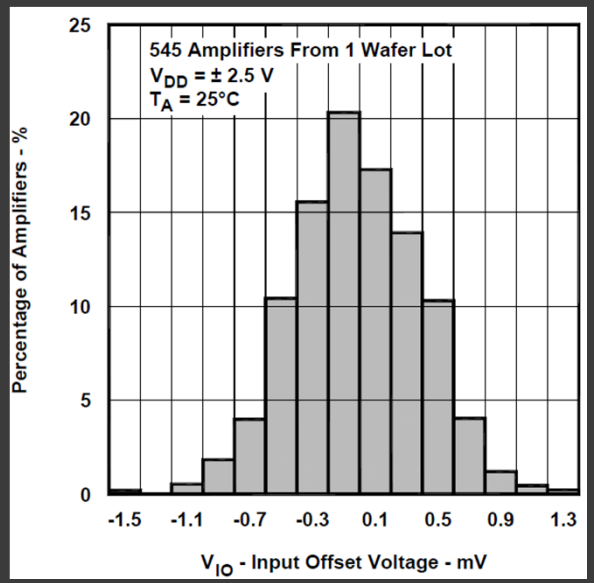
ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

DC Errors

Input Offset Voltage

- *Input Offset Voltage* is the voltage that must be applied to the input to make the output equal to zero volts
  - Polarity is not predictable as it is a manufacturing variance
- V_{os} ranges from a few μV to typ. around $5\ mV$
  - Chopper-stabilized are lowest ($< 1\ \mu V$)
  - "Precision" Op Amps have low V_{os}
  - Untrimmed CMOS amps can reach $50\ mV$
- V_{os} will drift with temperature and time
  - As low as $0.1\ \mu V/°C$, typically $1 - 10\ \mu V/°C$
  - Aging is proportional to the square root of time
    - $1\ \mu V/1000\ hr \rightarrow 3\ \mu V/year$ (9000 hours)
- Error due to Input Offset Voltage can be very large in Instrumentation Amplifiers



TVL2721 Spec:
0.5 mV typ, 3 mV max.

Errors resulting from Input Offset Voltage

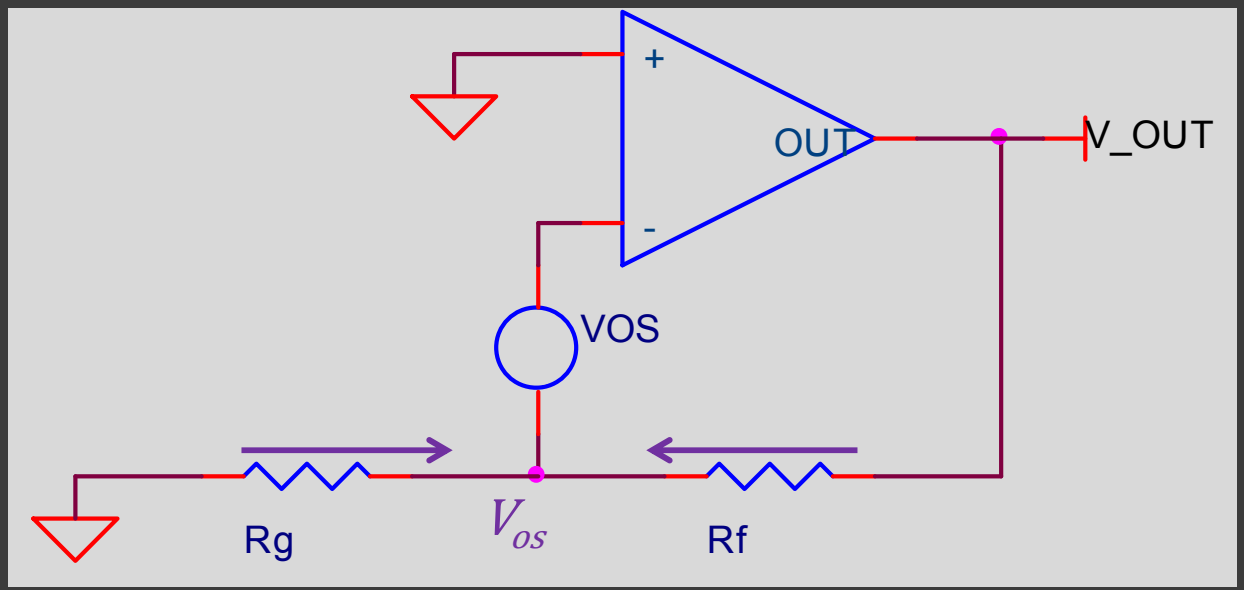
- Modeled as a voltage source in series with the inverting terminal
- Note: Inverting or Non-inverting result is the same

$$\frac{0 - V_{OS}}{R_g} + \frac{V_{OUT} - V_{OS}}{R_f} = 0$$

$$\frac{V_{OUT}}{R_f} = \frac{V_{OS}}{R_g} + \frac{V_{OS}}{R_f}$$

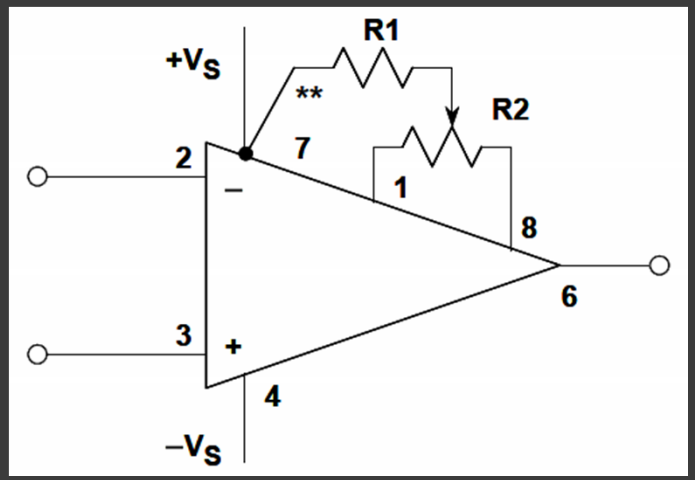
$$V_{OUT} = V_{OS}\left(1 + \frac{R_f}{R_g}\right)$$

$$V_{OUT} = V_{OS}\frac{1}{\beta}$$ ← Noise Gain (NG)



Nulling the Input Offset Voltage (internal)

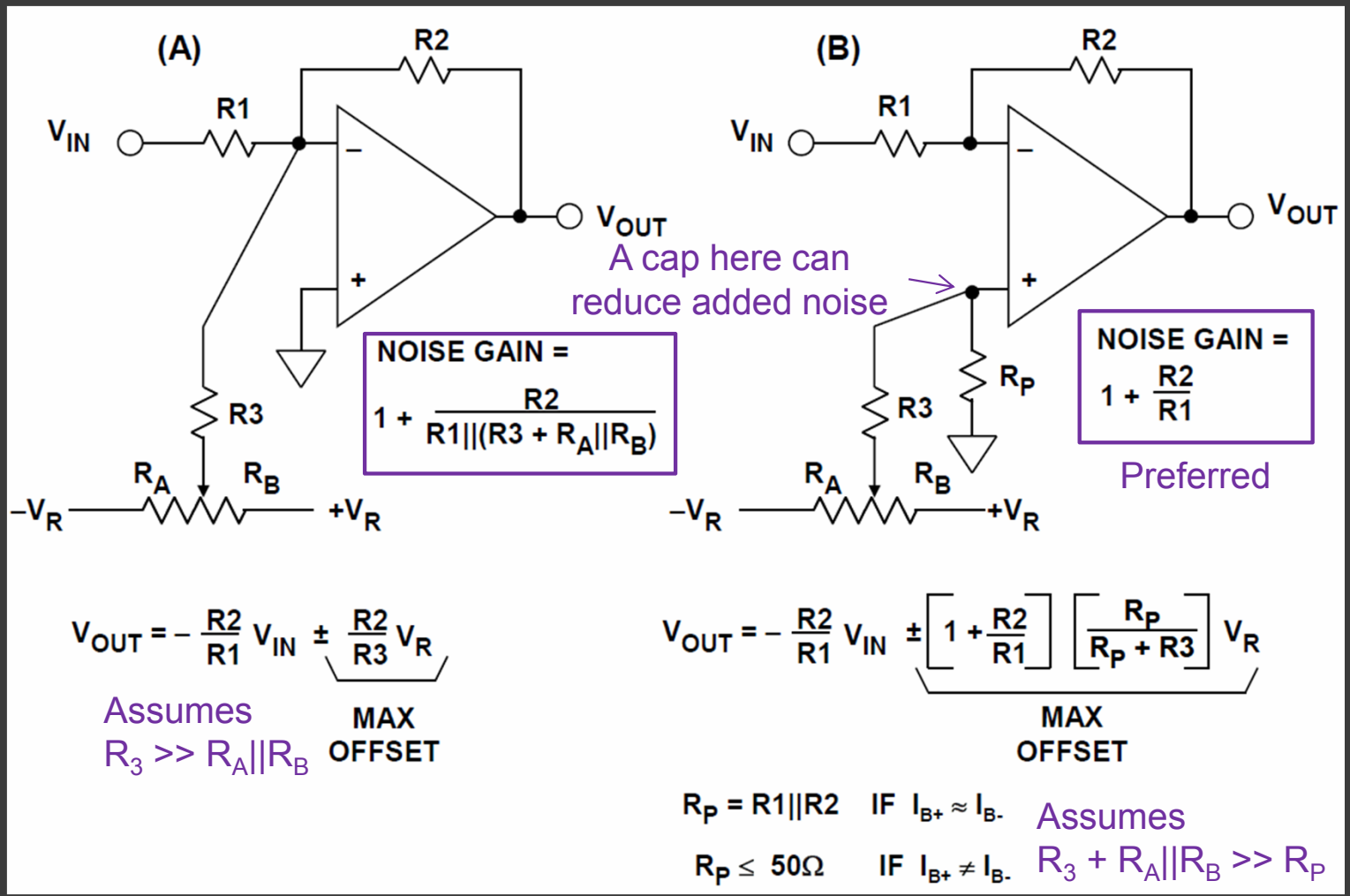
- Null or trim pins
  - Only for removing Op Amp offset
    - Do not use to correct system level errors
  - Topology depends on specific Op Amp
    - Read the data sheet!
  - Direct connection to differential pair
    - May have more gain than inputs
    - Use a tight layout for low-noise



- Null pin connections increases Op Amp temperature drift
- Generally, I avoid this method
  - Pots are generally poor devices (temperature effects, stability)
- Pick a “better” Op Amp if offset is a problem

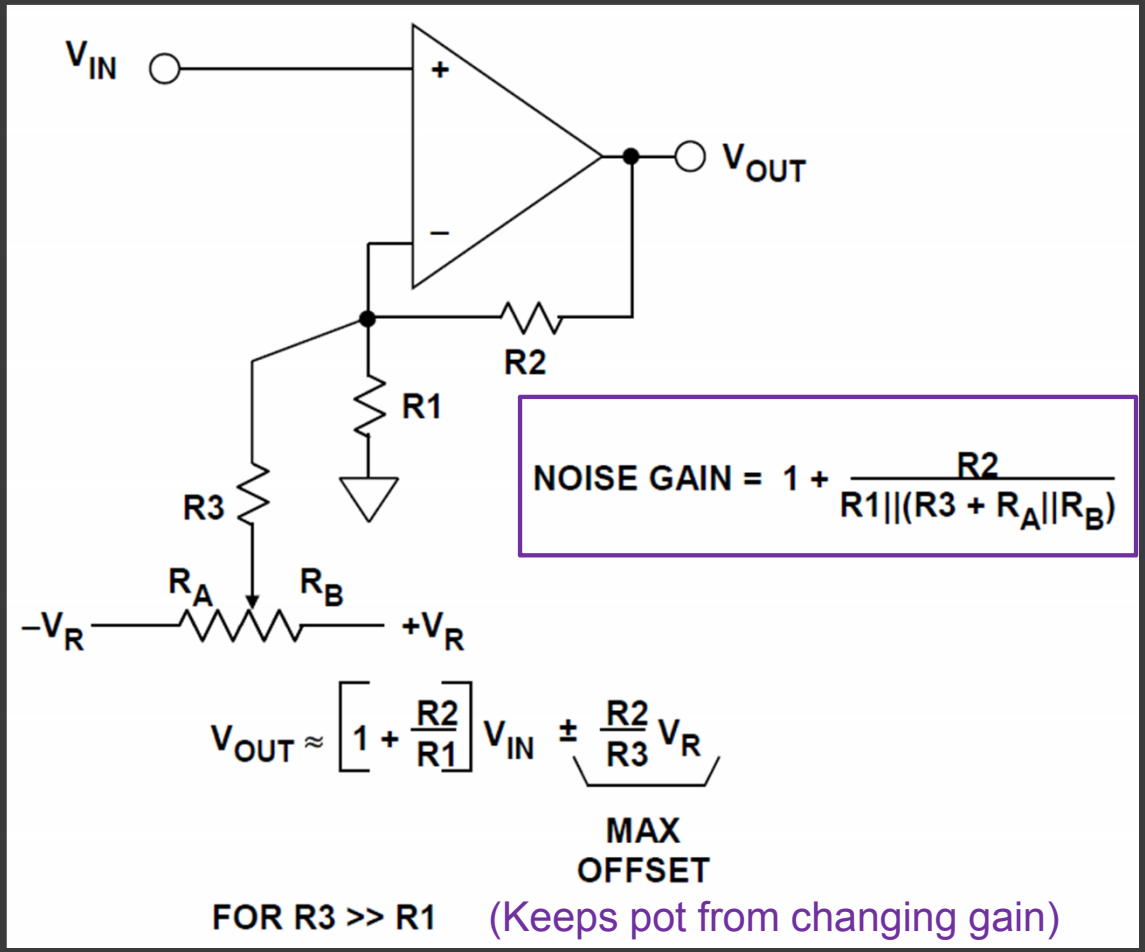
Nulling the Input Offset Voltage (external) Inverting amplifier

- Use a reference voltage (or a DAC), not the supply

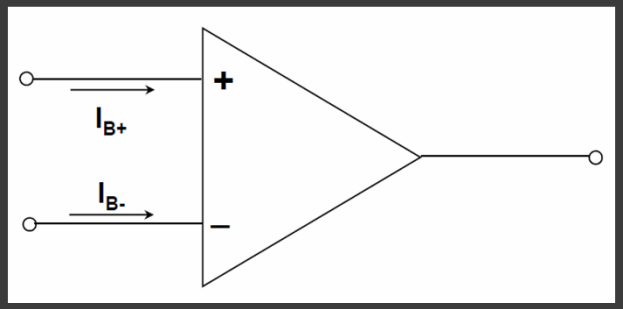


Nulling the Input Offset Voltage (external)
Non-inverting amplifier

- Pick components to minimize change in noise gain
- Pot/Reference can always be replaced by a DAC



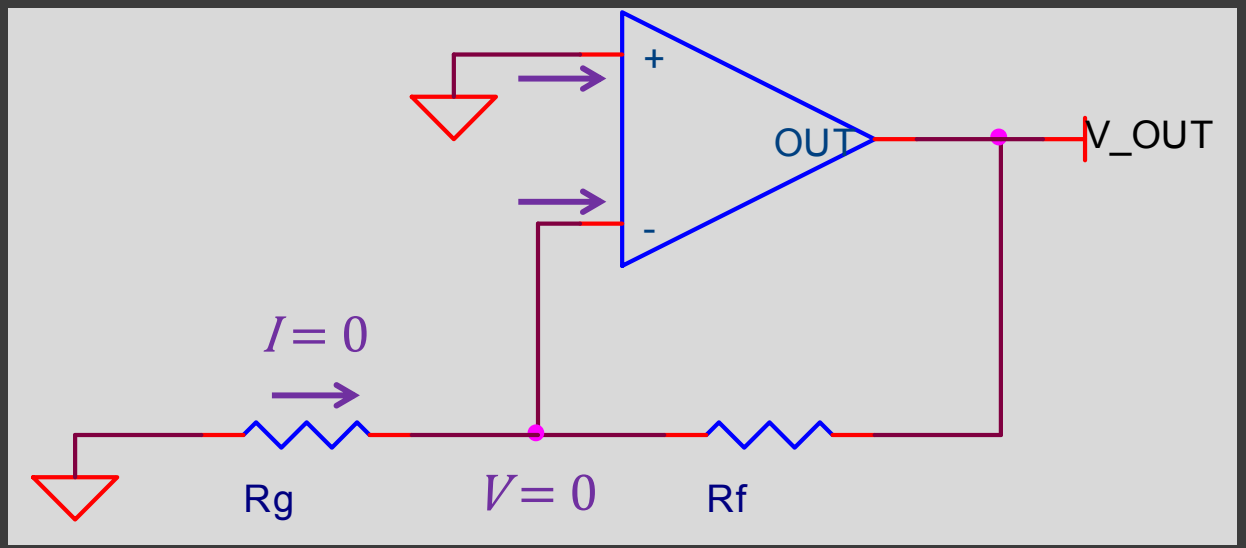
Input Bias Current



- As low as 60 fA to several μA
- Very variable
- Inputs can be well-matched…or not
- Can be stable with temperature or may double every 10 °C
- May flow in or out and can change direction with CM voltage
  - Depends on input structure and internal cancellation circuits
- Don't assume that both inputs currents flow the same direction
  - Look at Input Offset Current specification
    - I_{os} is the difference between I_{bias+} and I_{bias-}
    - If I_{os} << I_{bias} currents probably flow the same direction
    - I_{os} is meaningless for current feedback amplifiers
- Pick a "better" opamp

Errors resulting from Input Bias Current (I)

- I_{bias+} contributes nothing because there is no resistance for it to flow through to convert it to a voltage
- I_{bias-} flows through R_f so $V_{out} = R_f I_{bias-}$
  - Note: direction of current flow is assumed – depends on internal structure

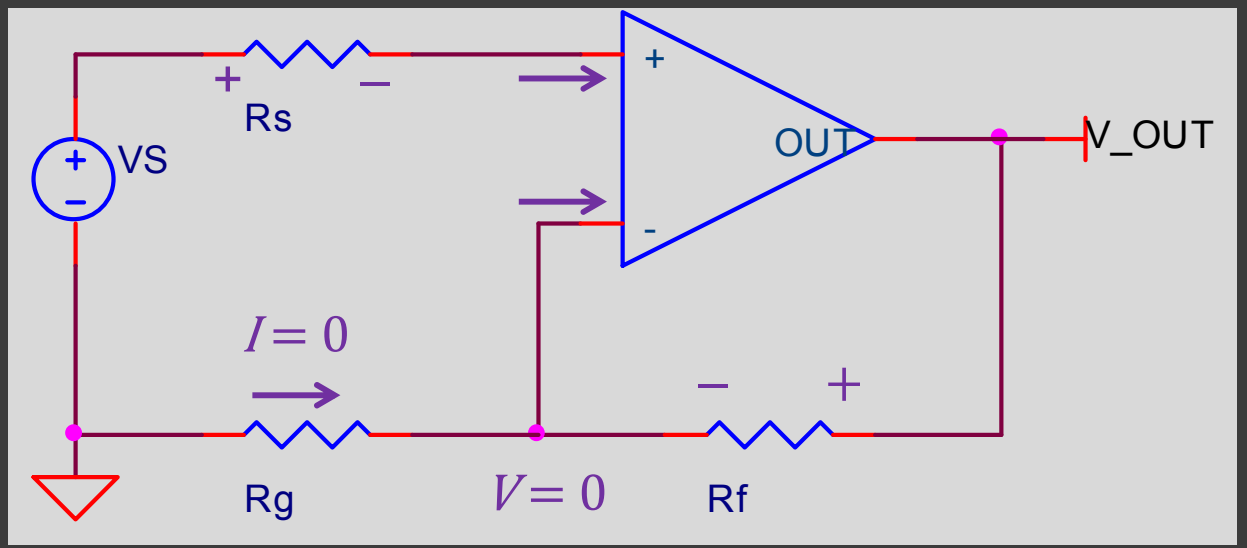


Errors resulting from Input Bias Current (II)

- Addition of R_s converts I_{bias+} to a voltage that sees the amplifier's non-inverting gain
- I_{bias^-} still flows through R_f
- Again: direction of current flow is assumed

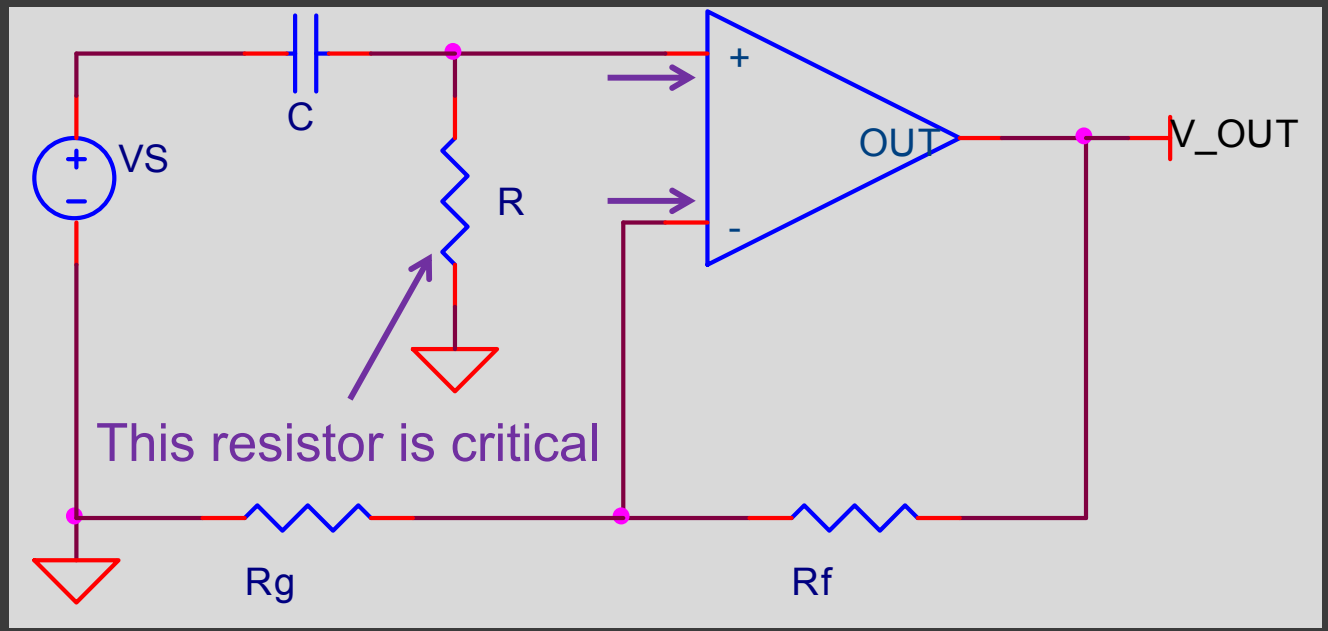
$$V_{OUT} = R_f I_{bias-} - R_s I_{bias+}\left(1 + \frac{R_f}{R_g}\right) + V_s\left(1 + \frac{R_f}{R_g}\right)$$

DC error due to input bias currents



Watch out for AC coupled circuits

- Op Amp inputs must have a DC part to ground
  - Applies to Instrumentation amps too!
- Without R, non-inverting node will drift until V_{out} saturates
  - For polarity shown, output will go to the negative rail
  - Time required: $dV/dt = I_{bias+}/C$



Cancelling the effects of Input Bias Current

- Recall the previous equation and set $V_s = 0$

$$V_{OUT} = R_f I_{bias-} - R_s I_{bias+}\left(1 + \frac{R_f}{R_g}\right)$$

- Proper selection of R_s will result in the cancellation of the errors caused by the Input Bias Currents

$$R_f I_{bias-} = R_s I_{bias+}\left(1 + \frac{R_f}{R_g}\right)$$

$$R_s = \frac{R_f}{1 + \frac{R_f}{R_g}} = \frac{R_f}{\frac{R_g + R_f}{R_g}} = \frac{R_f R_g}{R_f + R_g} = R_f \| R_g$$

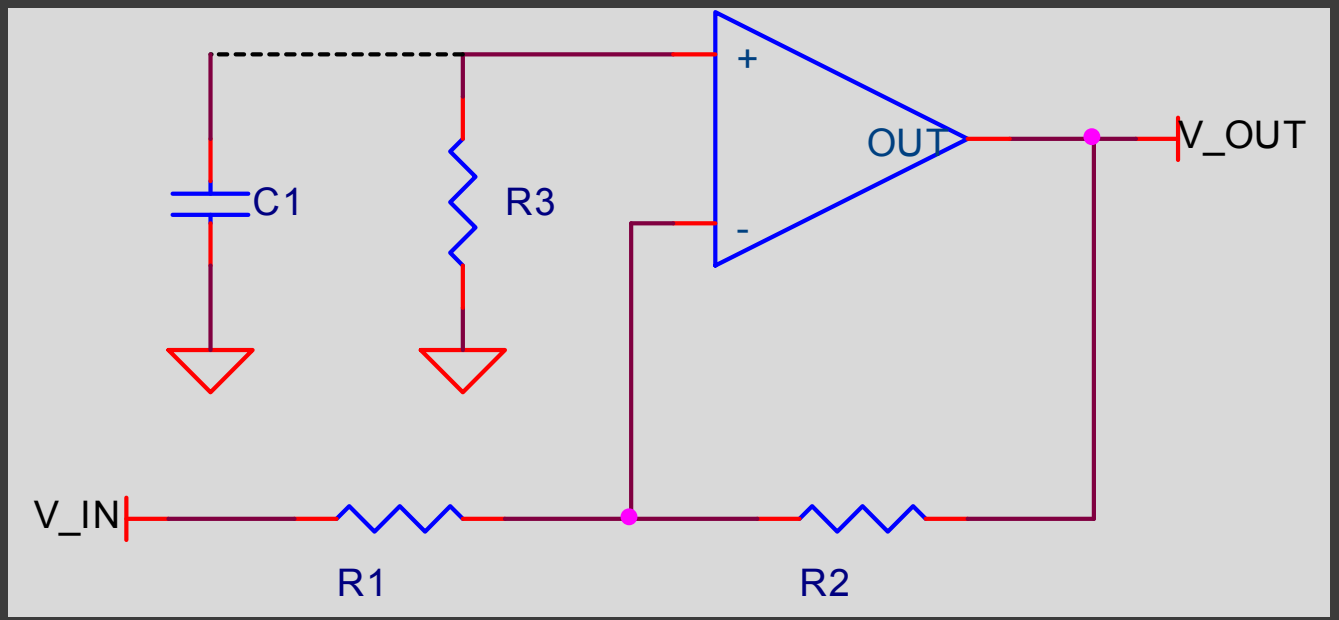
- Lots of assumptions!

Requirements for Input Bias Current Cancellation

- Cancellation technique only works when Input Bias Currents are well matched
  - I_{bias+} and I_{bias-} must be (nearly) equal and flow in the same direction
- Key is to look at the Input Offset Current specification
  - Input Offset Current must be << Input Bias Current
    - Op Amps with internal bias current compensation have $I_{os} \approx I_{bias}$
  - Watch out for Rail-to-rail Op Amps
    - Direction can change with common-mode voltage
- If not well matched, this technique makes the error worse
- If you don't know what you are doing…don't try designing it
  - Or build the circuit and learn something!

Input Bias Current Cancellation Circuit

- Cancellation technique only works when Input Bias Currents are well matched
- Pick $R_3 = R_1 \,||\, R_2$
- C_1 is for noise reduction (discussed in a later lecture)
- Circuit still has an error from V_{os}



Output Drive

- Op Amp output swing is limited by load
- Most Op Amps can output 10 mA
  - If you need more, look closely at specs or add a current booster
- Greater loading can change performance
  - Increased distortion
  - Higher temperature (due to power dissipation)

OPA177 SPECIFICATIONS

At V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITION	OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT VOLTAGE RANGE								
Common-Mode Input Range[4]		±13	±14		*	*		V
Common-Mode Rejection	V_{CM} = ±13V	130	140		115	*		dB
OPEN-LOOP GAIN	$R_L \geq 2k\Omega$							
Large Signal Voltage Gain	V_O = ±10V[5]	5110	12,000		2000	6000		V/mV
OUTPUT								
Output Voltage Swing	$R_L \geq 10k\Omega$	±13.5	±14		*	*		V
	$R_L \geq 2k\Omega$	±12.5	±13		*	*		V
	$R_L \geq 1k\Omega$	±12	±12.5		*	*		V
Open-Loop Output Resistance			60			*		Ω

Slew Rate

- Large-signal AC parameter affecting output voltage
  - Maximum dV_{out}/dt the output can support
  - Dictated primarily by internal Miller compensation capacitor
- Differential input voltage can be large when slew-rate limited
- Full-power bandwidth ($FPBW$) is set by the SR specification
  - Maximum full-amplitude sinusoid ($\pm V_p$) that can be output without slew rate limiting

$$FPBW = \frac{SR}{2\pi V_p}$$

- $FPBW$ is typically much less than f_τ (A_v unity gain frequency)
  - OP-27 has $8\ \mathrm{MHz}$ small signal bandwidth and $32\ \mathrm{kHz}$ FPBW
  - "Small-signal" amplitude (output) can be as low as $\pm\ 100\ \mathrm{mV}$

Input and Output Impedance

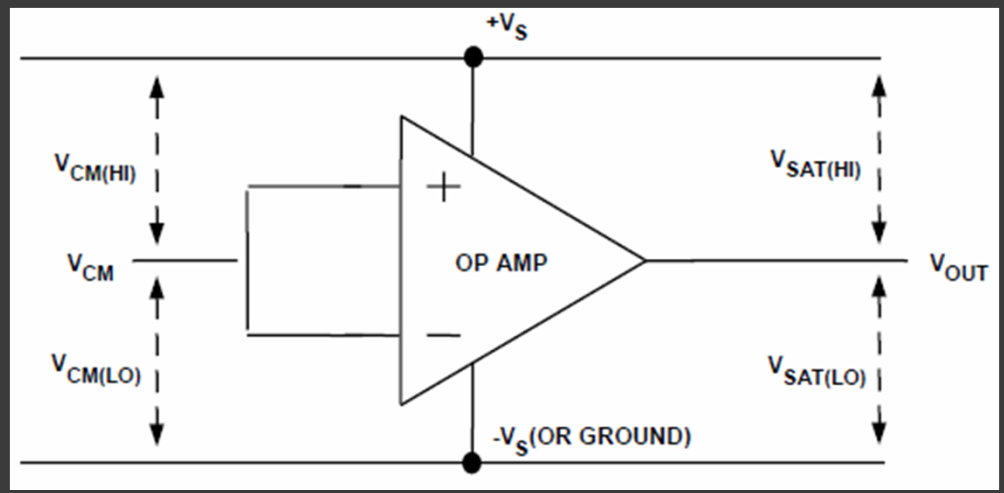
- Op Amp input impedance is typically a large resistance in parallel with a small capacitance
  - 10^5 – 10^{12} Ω || 3 – 25 pF
  - CM impedance is from each input to ground
  - DM impedance is between inputs
  - BJT input stages typically have lower capacitance
  - CM input voltage can modulate input capacitance in non-inverting amplifiers and cause distortion
- Op Amp output impedance is typically treated as a resistance
  - 10 – 100 Ω is typical, can be 1 kΩ
  - Reduced by $(1 + A_v\beta)^{-1}$ in closed loop designs
  - Can be an issue at high frequencies when $A_v\beta$ craps out
  - Can be an issue with capacitive loads

Input and Output Common Mode Range

- Input Common Mode Voltage is defined as:

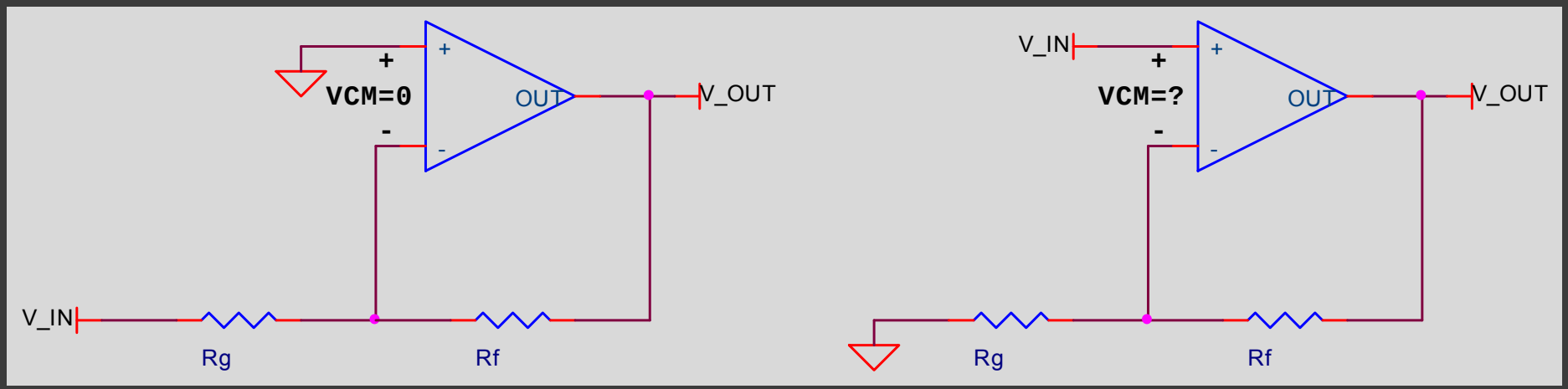
$$V_{ICM} = \frac{V_{IN+} + V_{IN-}}{2}$$

- More important is the input and output common mode range
  - The common-mode range is specified w.r.t the supply voltage
  - Defines how close the input or output can get to the rail before saturating
- Watch out for rail-to-rail
  - Last 50 mV is often nonlinear
- Single supply design!



Interesting Common Mode Issue

- Op Amps have differential mode and common mode gain
  - High DM Gain (A_v)
  - Low CM gain, aka high CM rejection (CMR)
- Instrumentation amplifiers and difference amplifiers are designed for very high CMR
  - 80 dB to 140 dB rejection is possible
- Not all amplifier configurations are created equal
  - Non-inverting amp sees large CM voltage → distortion due to CM gain



Op Amp Model (up to this point)

- Superposition allows you to analyze individual effects
- R_i and R_o are actually complex impedances

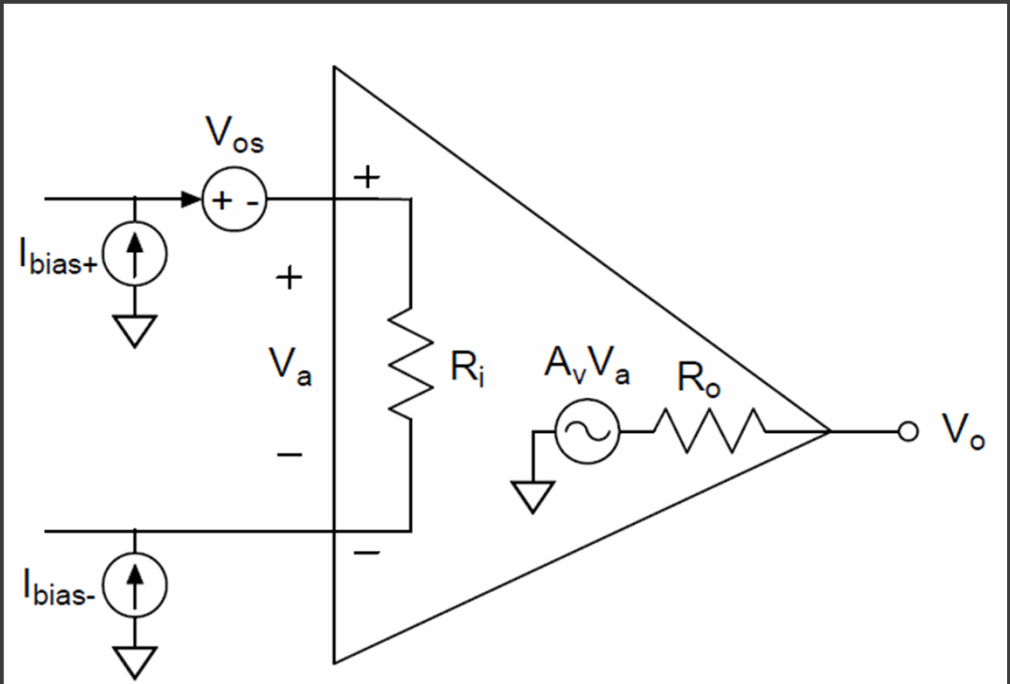
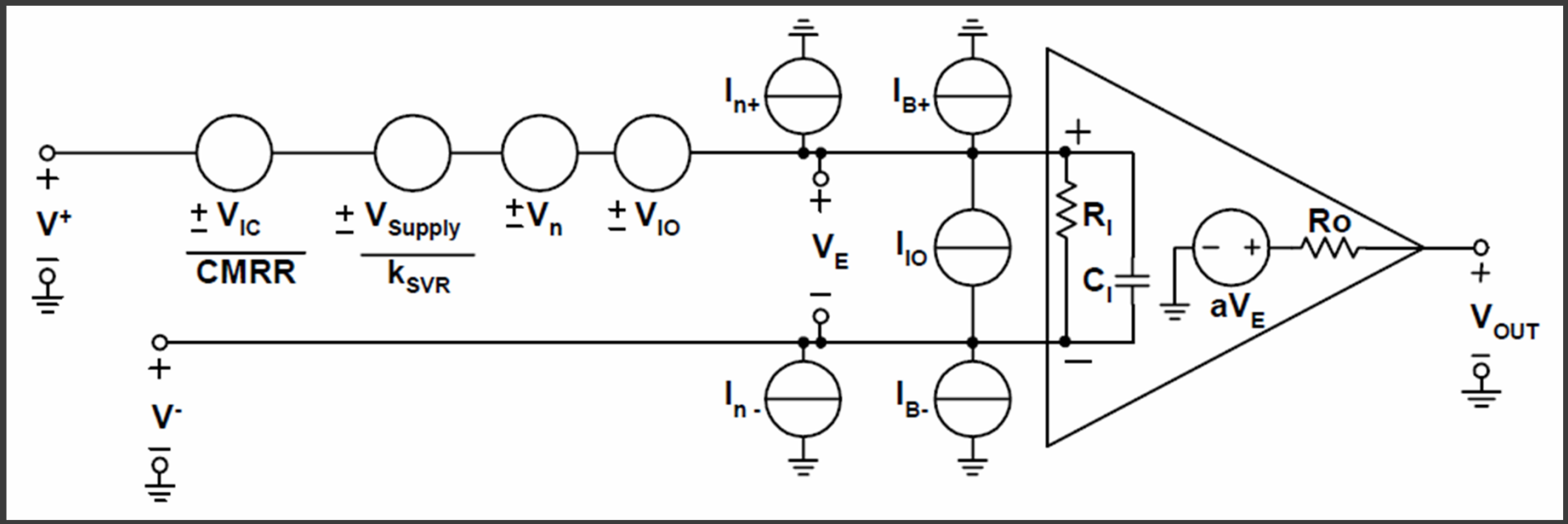


Figure 5. Op Amp model including common parameters.

Source: "*Technote 7 – Using Op Amps Successfully*", Tim J. Sobering, 2006

Full Op Amp Model (inc. noise sources)



Single Supply Design

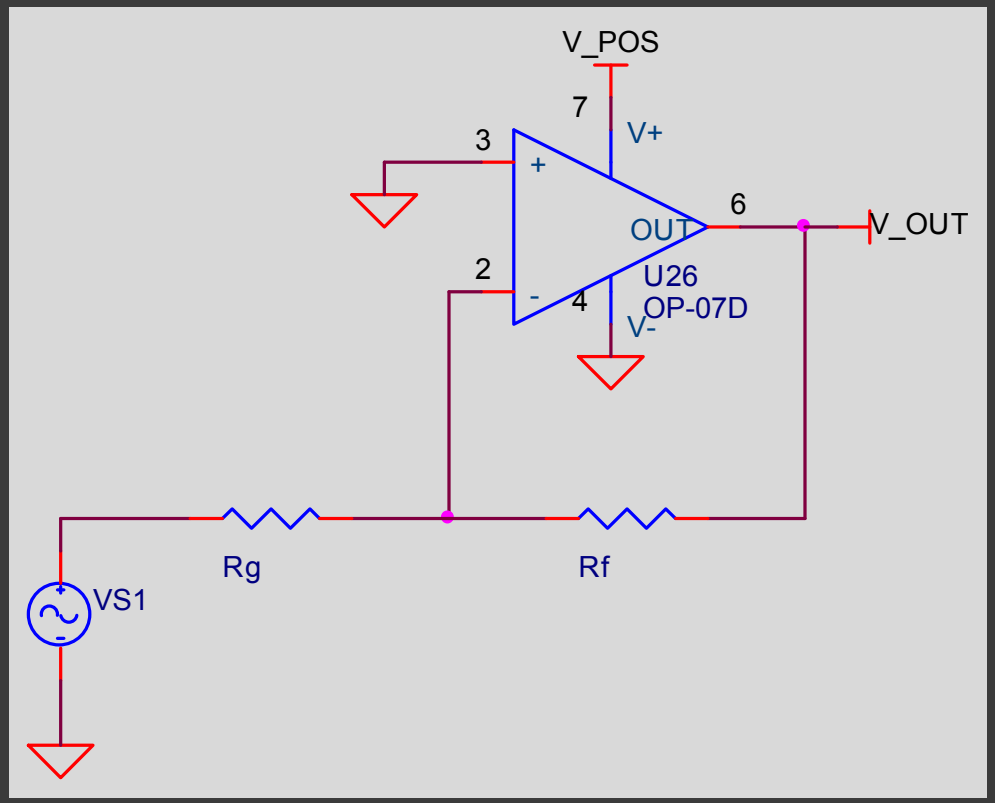
- No such thing as single supply…sort of
  - Op Amps do not have a ground terminal
    - LM324 has a ground pin! (not really)
  - Any Op Amp can be operated with a single-supply
- Single supply operation requires proper input biasing and output interfacing
  - Avoid common mode range violations
  - Don't accidentally amplify DC levels
    - Multi-stage DC coupled designs are tricky
- So why are some Op Amps called single-supply?
  - Rail-to-rail inputs and/or output
  - CMR includes one or both rails
  - Often low-power and/or low-supply voltage

Single Supply Design Issues

- Lowered supply rails:
  - Reduced dynamic range (reduced noise margin)
  - Reduced precision because open-loop gain may be lower
  - Bias currents can change with reduced supply voltage
  - Offset voltage is impacted (PSRR)
  - Reduced output drive (needs “lighter” loads)
- Example of how reduced supply affect an Op Amp:
  - OP177 has initial offset of $\pm$ 20 μV at $\pm$ 15V with a PSRR of 1 μV/V (-120 dB – Power Supply Rejection Ratio)
  - At $\pm$ 5V, 20V reduction in supply changes offset by $\pm$ 20μV
  - New offset voltage spec is $\pm$ 40μV
- Rail-to-rail inputs and outputs suffer linearity issues
  - May not actually get to the rail – 50 mV seems to be common value
  - Generally, the last 50 – 100 mV before saturation is non-linear

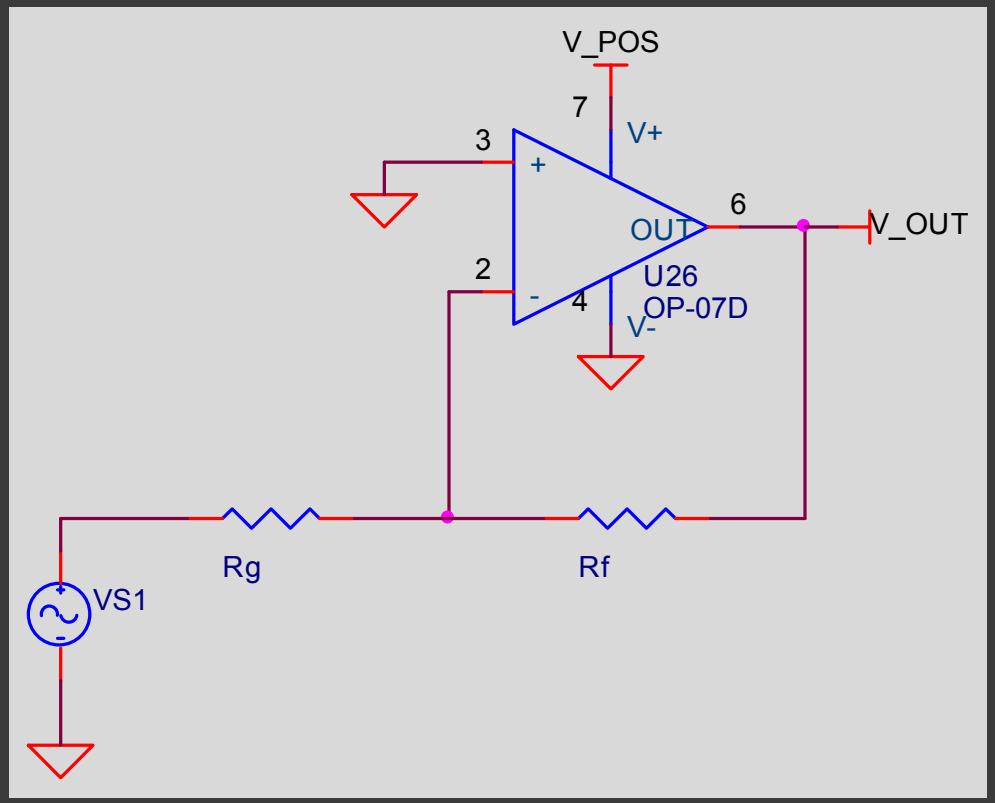
Selection/design of “ground” reference is critical

- Is there a problem?



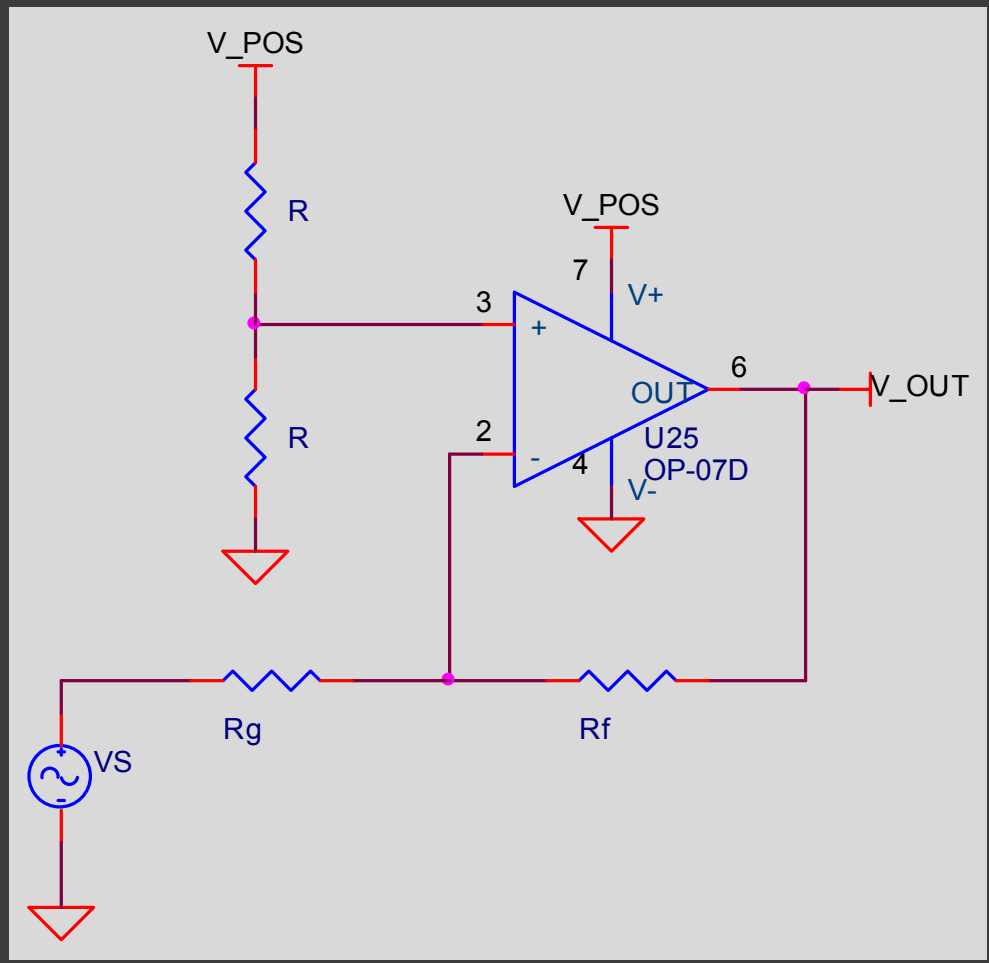
Circuit will only marginally function

- Output cannot go negative when input is positive
- Output will have a small “dead-band” when going positive (~1.5V for OP-07)
- RRIO Op Amp reduces but doesn’t eliminate the problems



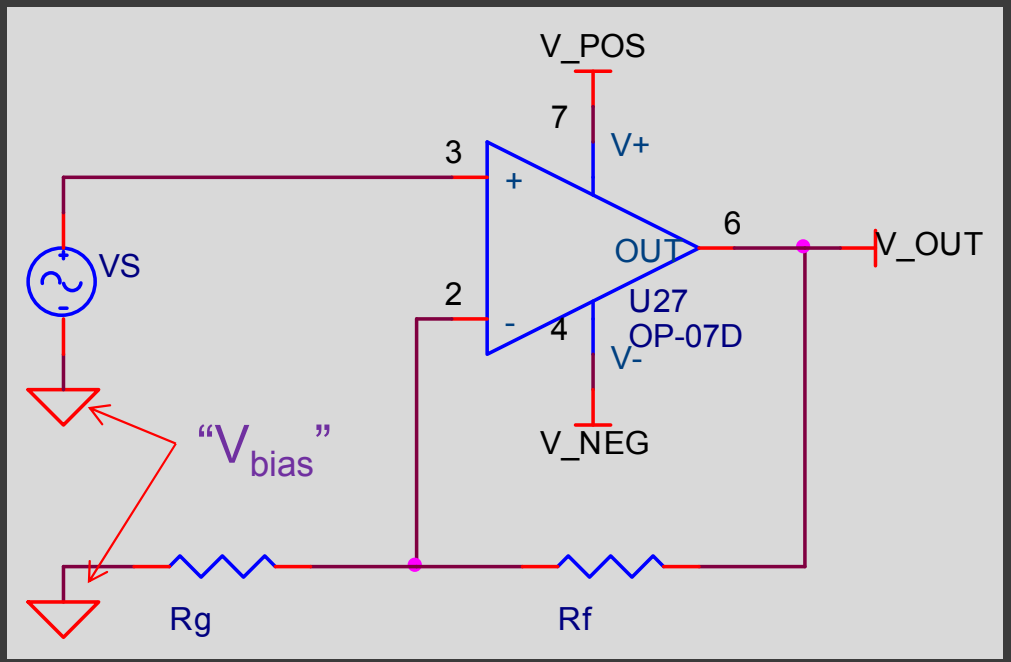
So lets bias the input away from the negative rail…

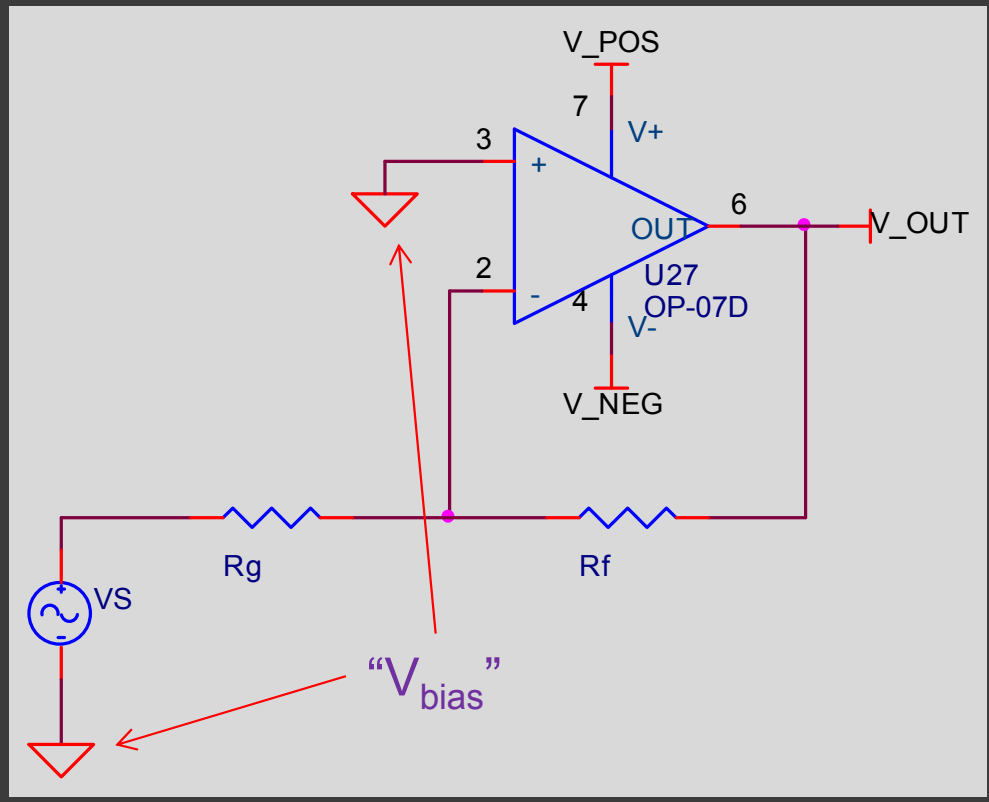
- Feedback will force inverting node to $V_{pos}/2$
  - Progress – it might be inside the CMR
- V_s "sees" the inverting gain $-R_f/R_g$
- But…
  - Voltage on non-inverting terminal sees positive gain, so output could be saturated
  - Output only swings when input pulls output away from positive rail
  - Operation is still marginal



Go back to the basics

- Op Amp doesn't know what "ground" is
- "Ground" nodes are "biased" to $V_{bias} = (V_{pos} + V_{neg})/2$
  - It just "happens" to be 0 V

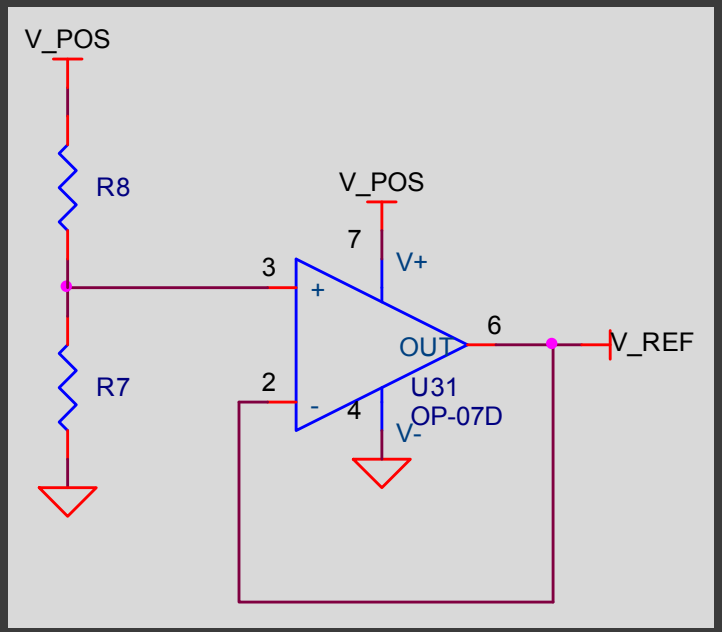




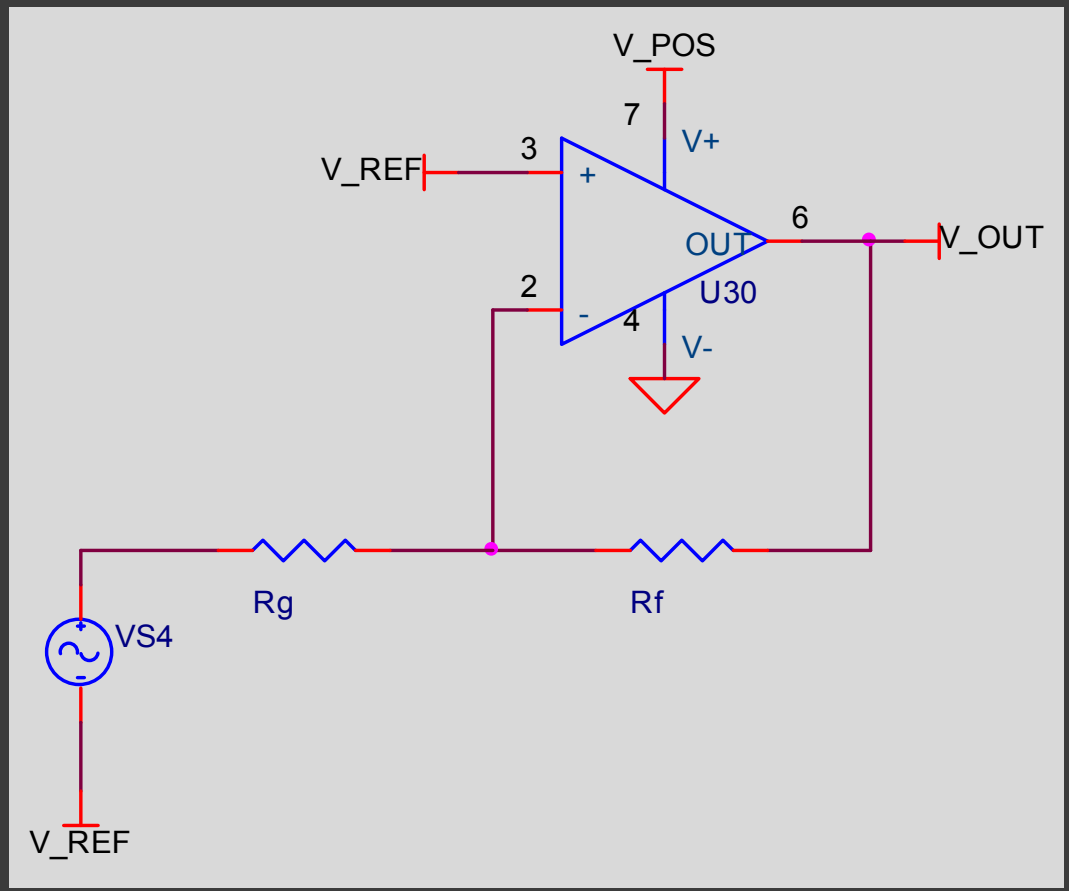
- So we can make a single supply design work by mimicking this biasing

Single Supply Alternatives

- Replace “ground” with V_{REF}
- Make sure V_{REF} is a low-impedance source



Low-impedance reference



When in doubt, do the math!

- Replace "ground" with V_{REF}

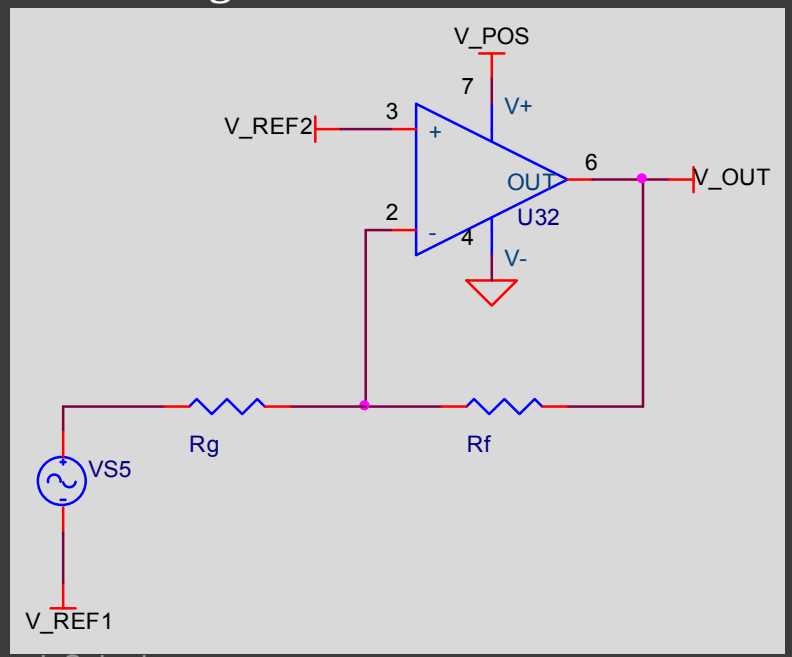
$$V_{out} = \left(1 + \frac{R_f}{R_g}\right) V_{REF2} - \frac{R_f}{R_g}(V_s + V_{REF1})$$

$$V_{out} = V_{REF2} + \frac{R_f}{R_g}(V_{REF2} - V_{REF1}) - \frac{R_f}{R_g} V_s$$

If $V_{REF1} = V_{REF2} = V_{REF}$

$$V_{out} = V_{REF} - \frac{R_f}{R_g} V_s$$

- Output swings relative to V_{REF}



Key points for Single-Supply Design

- Don’t inadvertently amplify your DC bias
- Extra biasing resistors can add noise
  - Use filtering caps if not in signal path
- AC coupling works when biased correctly and DC response isn’t needed
- Make sure your reference has a low source impedance
  - Source impedance can change circuit gain
- Watch out for CMR violations

Questions?